Hybrid Full-Bridge Converter with Low Switching Loss and Freewheeling Current

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Abstract—**This paper presents a soft switching converter with the advantages of wide zero-voltage switching range, low primary conduction loss, less output inductance and power transfer within the whole switching cycle. Half-bridge circuit is connected to the lagging-leg power switches of full-bridge converter to improve the soft switching load range. Passive snubber is connected on the secondary side of full-bridge converter. One positive rectified voltage is generated on the secondary side in order to reduce the primary current to zero during the freewheeling state. Therefore, the primary conduction loss is reduced. Since the output inductor voltage at the freewheeling state is also decreased, the output inductance of full-bridge converter can be reduced. The output sides of the full-bridge converter and the half-bridge converter are series connection so that the proposed converter delivers energy from the input voltage to the output load within the whole switching period. The performance of the proposed converter is verified by the experimental verifications with a 1.92*k*W prototype.**

Keywords—Full-bridge converter, zero-voltage switching, freewheeling current, passive snubber.

I. INTRODUCTION

High efficiency power converters have been demanded in modern power units. Low output voltage with high output current and high reliability is necessary for these applications. Resonant converters based on *LLC* topology [1-4] and full-bridge converters [5-7] have been proposed to achieve low switching losses and high circuit efficiency. *LLC* resonant converters have the advantages of high circuit efficiency at high input voltage, wide range of zero-voltage switching (ZVS) operation and possible no reverse recovery current of the rectifier diodes. However, the drawbacks of the *LLC* converters are wide frequency variation due to the wide input voltage and load current range and high circulating current losses due to the low inductor ratio between the magnetizing inductance and the series resonant inductance. Therefore, the power rating of the half-bridge and full-bridge *LLC* converter is mostly limited at 600W and 1200W output power, respectively. Full-bridge converters have the advantages of high power output and wide ZVS range of the leading-leg switches due to the energy stored on the output filter inductor. However, the main weaknesses of conventional full-bridge converters are high circulating current at the commutation interval and narrow ZVS range of the lagging-leg switches due to the limited energy stored on the transformer leakage inductor. Passive snubber circuits [8] have been presented on the secondary side to achieve zero-current switching (ZCS) turn-off of the lagging-leg switches and reduce the voltage spike across the rectifier diodes. The large leakage inductance or an external resonant inductance [9] is connected on the primary side to increase the ZVS range at the lagging-leg. The drawbacks of these approaches are high duty cycle loss on these circuit topologies and low effective duty cycle. The auxiliary circuits are added on the primary side of transformer in [10] to extend ZVS range.

A new DC/DC converter with the features of wide ZVS range for the lagging-leg switches and low primary current at the commutation interval is proposed to overcome the drawbacks of the conventional full-bridge converters. A full-bridge converter and a half-bridge converter with sharing the lagging-leg switches is adopted in the proposed circuit to transfer energy during the whole switching period. The energy stored on the output inductor of a half-bridge converter is adopted to increase ZVS range of the lagging-leg switches. Thus, the narrow ZVS range at the lagging-leg switches in the conventional full-bridge converters is improved. Passive snubber is connected on the secondary side of the full-bridge converter to generate a positive voltage at the freewheeling state in order to reduce the primary current to zero. Finally, the performance of the proposed converter is demonstrated by experiments with 1920W prototype.

II. CIRCUIT DIAGRAM

In the conventional full-bridge converters with medium power applications, the phase-shift pulse-width modulation is used to regulate the output voltage and achieve the ZVS operation of power switches. However, the problems of the conventional full-bridge converters are high circulating current at freewheeling state, less ZVS operation range at the lagging-leg switches and low circuit efficiency at light load. These problems can be improved in the proposed converter and the circuit configuration of the adopted circuit is given in Fig. 1. The adopted circuit includes a full-bridge converter (V_{in}, S_1-S_4, C_{S1}-C_{S4}, T_1, L_{r1}, D_1, D_2, L_{o1} and C_{o1}) and a half-bridge converter (V_{in}, S_3, S_4, C_{S3}, C_{S4}, T_2, L_{r2}, C_r, D_3, D_4, L_{o2} and C_{o2}) to transfer power from V_{in} to R_o during the whole switching period. The ZVS turn-on of power switches S_1 and S_2 in leading-leg are achieved by using the energy stored in L_{r1} and L_{o1} to discharge C_{S1} and C_{S2}. The ZVS turn-on of S_3 and S_4 are achieved by using the energy stored in L_{r1} and L_{r2} and the magnetizing current i_{Lm2} to discharge C_{S3} and C_{S4}. Therefore, S_1-S_4 can be turned on at ZVS from light load to full load. The half-bridge converter works at constant duty cycle and the output voltage V_{o2} is un-regulated. Passive snubber circuit, C_c, D_a and D_b, is

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connected at the secondary side to provide a positive voltage instead of zero voltage at the rectified voltage v_r. During the freewheeling duration, the rectified voltage v_r=v_{Cc} and the output inductor voltage v_{Lo1}=v_{Cc}-v_o instead of -v_o. This positive voltage is reflected to primary side to reduce the primary current i_{p1} to zero. Thus, the high conduction loss at the freewheeling state in conventional full-bridge converter is improved and the circuit efficiency is increased. The output inductor size of L_{o1} is also reduced. The output voltages V_{o1} and V_{o2} are series connection so that half-bridge converter can transfer energy from V_{in} to R_o during the whole switching cycle and full-bridge converter can transfer energy to output load during the active states, S_1 (S_2) and S_4 (S_3) on.

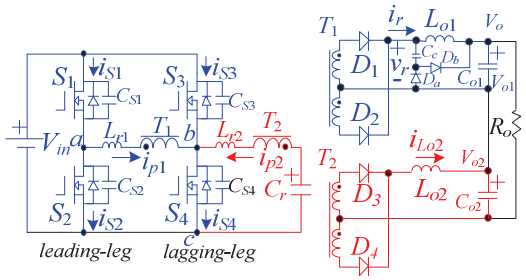


Fig. 1 Circuit diagram of the proposed circuit.

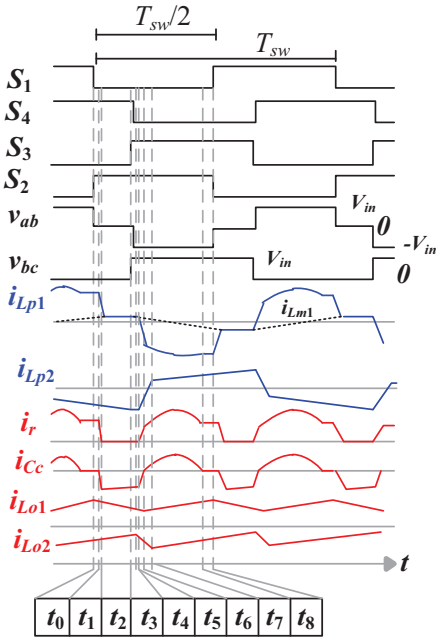


Fig. 2 Main PWM waveforms during one half of a switching cycle.

III. Operation Principles

In order to achieve the wide ZVS operation of all switches, the phase-shift PWM is used to control the adopted converter. Fig. 2 illustrates the main PWM waveforms during one switching cycle. S_1 and S_2 are in the leading-leg and S_3 and S_4 are in the lagging-leg. There is a phase shift angle between the leading-leg and lagging-leg to regulate the output voltage V_o. All power semiconductors and passive components are assumed to be ideal. The turn ratios of T_1 and T_2 are n_1 and n_2, respectively. Due to the conduction states of all power semiconductors, there are nine operation stages in each half of the switching period. Since the PWM waveforms in each half cycle are symmetry, only first nine stages are discussed and analyzed as follows. The topological circuits for the first switching period are given in Fig. 3. Before t_0, S_1, S_4, D_1 and D_4 are conducting and the primary currents i_{p1}>0 and i_{p2}<0.

Stage 1 [t_0 - t_1]: Power switch S_1 is turned off at time t_0. Since the primary current of the full-bridge converter i_{p1} is positive, capacitor C_{S2} is discharged. The energy stored in L_{r1} and L_{o1} can be used to discharge C_{S2} to zero at time t_1.

Stage 2 [t_1 - t_2]: At time t_2, capacitor C_{S2} is decayed to zero voltage. Since the primary current $i_{p1}(t_1)$ is positive, the anti-parallel diode of S_2 conducts and the ZVS turn-on of S_2 is achieved after t_1. When t>t_1, the rectified current i_r of the full-bridge converter is less than the output inductor current i_{Lo1}. In this stage, the clamped diode D_a conducts, v_r=v_{Cc}, v_{Lo1}=v_{Cc}-V_o<0, and i_{Lo1} decreases. The primary voltage of T_1 equals n_1v_{Cc}, v_{Lr1}=-n_1v_{Cc}, and i_{p1} is decreased to zero at time t_2. In the conventional full-bridge converter, the primary current is kept at $i_{p1}(t_1)$ during the freewheeling state. Therefore, there is a large conduction loss at this freewheeling state. However, the primary current of the adopted circuit is decreased to zero at the freewheeling state due to the positive rectified voltage at the secondary side. Thus, the circuit efficiency of the adopted circuit can be improved.

Stage 3 [t_2 - t_3]: At time t_2, the secondary rectified current i_r=0 so that the primary side current of the full-bridge converter i_{p1} is equal to the magnetizing current i_{Lm1}. In this stage, the rectifier didoes D_1, D_2 and D_3 are reverse biased and the output inductor current i_{Lo1} decreases. The energy stored in the clamped capacitor C_c is transferred to the output capacitor C_{o1}. The half-bridge converter continuously transfers energy from C_r to C_{o2} and the output inductor current i_{Lo2} increases.

Stage 4 [t_3 - t_4]: Power switch S_4 is off at time t_3. The primary side currents $i_{p1}(t_3)$ and $i_{p2}(t_3)$ discharge C_{S3} and charge C_{S4}. This stage ends at time t_4 when capacitor C_{S4} is equal to v_{Cr}.

Stage 5 [t_4 - t_5]: At time t_4, the capacitor voltage is charged to v_{CS4}=v_{Cr}. Thus, the primary magnetizing voltage v_{Lm1}=0 and diodes D_3 and D_4 are both forward biased. The inductor voltage v_{Lo2}=-V_{o2} and i_{Lo2} decreases in this stage. The energy stored in L_{r2} and the magnetizing inductor current i_{Lm2} are used to discharge C_{S3} to zero voltage and charge C_{S4} to V_{in} in this stage.

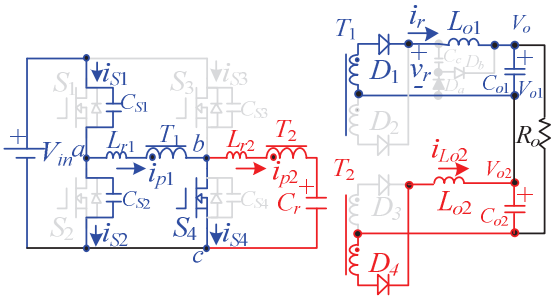
Stage 6 [t_5 - t_6]: Capacitor C_{S3} is discharged to zero voltage at time t_5. At t_5, i_{p1}-i_{p2}<0. The anti-parallel diode of S_3 is forward biased. Thus, S_3 can be turned on at this moment to reach ZVS. Since n_2i_{p2}<i_{Lo1}, diodes D_3 and D_4 are still in the commutation state. The primary currents i_{p1} and i_{p2} are decreased and increased, respectively. At time t_6, the secondary side current i_r equals i_{Lo1} and the diode current i_{Da} is zero. Switches S_2 and S_3 are in the on-state and the rectified voltage v_r equals v_{Cc}. No energy is transferred from V_{in} to V_{o1}.

Stage 7 [t_6 - t_7]: The primary current i_{p1} decreases until -i_{Lo1}/n_1 at time t_6. Then, the diodes D_a and D_b are reverse biased and forward biases, respectively. The reflected primary inductance $L_{r1}/(n_1)^2$ and C_c are resonant. The output inductor voltages v_{Lo1}=v_{Cc} and v_{Lo2}=-V_{o2} so that i_{Lo1} increases and i_{Lo2} decreases in this stage. The half of a resonant period, by $L_{r1}/(n_1)^2$ and C_c, is designed to be less than the effective duty cycle time of the

full-bridge converter. Thus, the capacitor current i_{Cc} can be decreased to zero before S_2 is turned off. In this stage, the primary current of full-bridge converter i_{p1}=-(i_{Lo1}+i_{Cc})/n_1. The half-bridge is still operated at the commutation state. This stage is ended at time t_7 when the commutation of the inductor current i_{Lo2} is completed. Then, the diode currents i_{D3}= i_{Lo2} and i_{D4}=0. In stages 5-7, S_2 and S_3 are conducting. However, the diodes D_3 and D_4 are conducting. No power is delivered from V_{in} to V_{o2}.

Stage 8 [t_7 - t_8]: At time t_7, the diode current i_{D4}=0. The full-bridge and half-bridge converters both transfer energy from input voltage to output load. The primary currents i_{p1} and i_{p2} are negative and positive, respectively. Both the output inductor currents i_{Lo1} and i_{Lo2} are increased in this stage. Since the half of the resonant period by $L_{r1}/(n_1)^2$ and C_c is less than the effective duty cycle time of the full-bridge converter, the rectifier current i_r will decrease to i_{Lo1} at time t_8. Then, the diode D_b is reverse biased.

Stage 9 [t_8 – t_9]: At time t_8, i_r=i_{Lo1} and i_{Cc}=0. The clamped diode D_b is reverse biased. In this stage, the output inductors are v_{Lo1}=V_{in}/n_1-V_{o1}>0 and v_{Lo2}≈(V_{in}-v_{Cr})/n_2-V_{o2}>0 so that i_{Lo1} and i_{Lo2} both increase. The stage ends at t_9 when S_2 is turned off. Then, the circuit operations of the first half of a switching period are completed.



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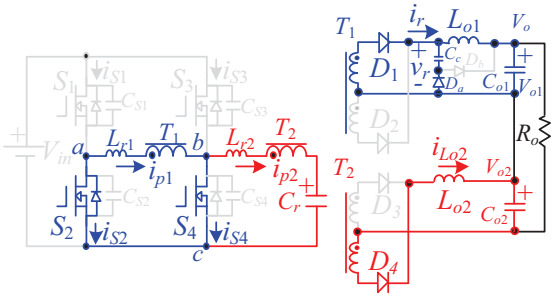

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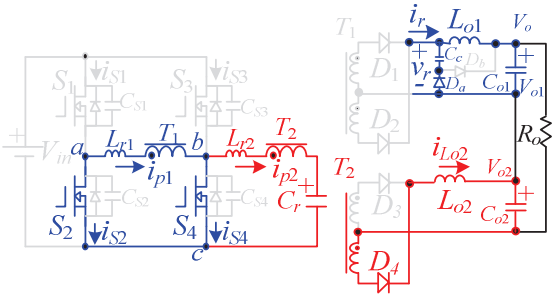

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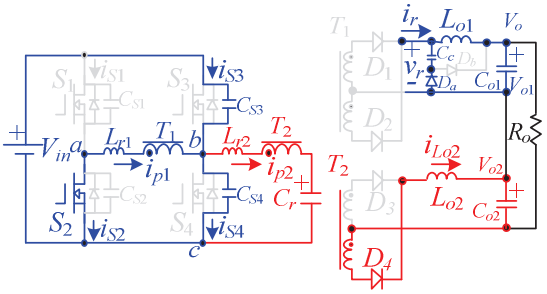

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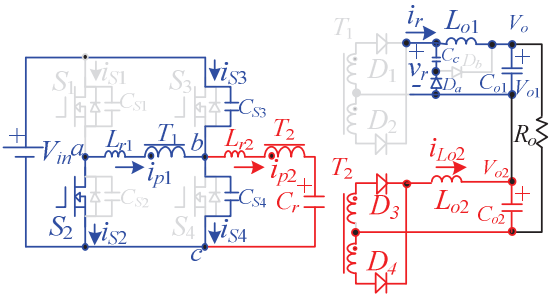

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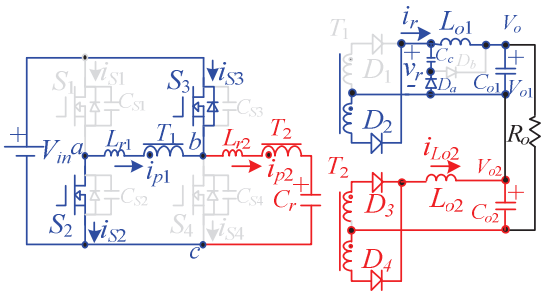

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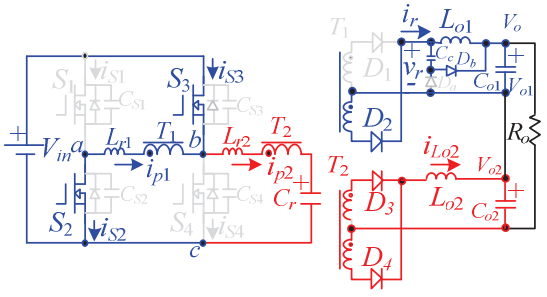

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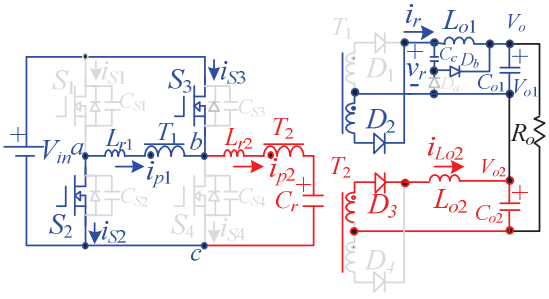

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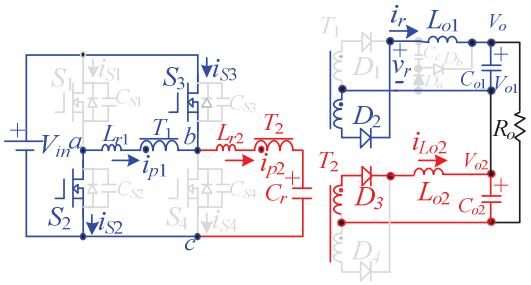

(i)

Fig. 3 Equivalent topological circuit in the first half of switching cycle (a) stage 1 (b) stage 2 (c) stage 3 (d) stage 4 (e) stage 5 (f) stage 6 (g) stage 7 (h) stage 8 (i) stage 9.

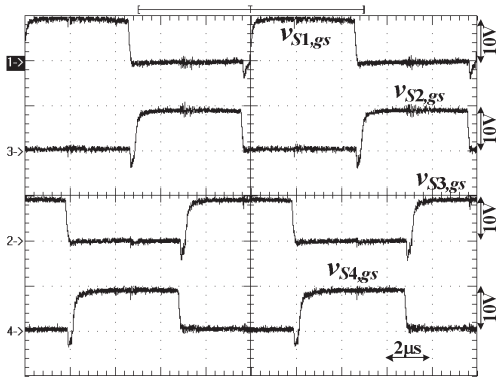

Fig. 4 Measured results of the gate voltages of S_1-S_4 at full load and V_{in}=400V.

IV. Experimental Results

The proposed converter is implemented with the following electric specifications V_{in}=350 V~400 V, V_o=48 V, P_o =1920 W, and f_{sw}=100 *k*Hz. The output power ratings of the half-bridge converter and the full-bridge converter are assumed as 800W and 1120W, respectively. The rated load current is 40A. The assumed output voltages are V_{o1}=28 V and V_{o2}=20 V. Experimental verifications based on the laboratory prototype are presented to verify the circuit performance. Fig. 4 gives the test waveforms of power switches. S_1 (S_3) and S_2 (S_4) have the complementary PWM waveforms. The PWM single of S_4 (S_3) is phase-shifted with respective to the signal of S_1 (S_2). Figs. 5-8 gives the measured PWM waveforms of switches S_1-S_4, respectively at light load. It is clear that the leading-leg switches S_1 and S_2 are all turned on under ZVS from 20% load and the lagging-leg switches S_3 and S_4 are all turned on under ZVS from 5% load. Compared to the conventional full-bridge converter, the ZVS of the lagging-leg switches in the adopted circuit is achieved from 5% load to full load. Fig. 9 illustrates the experimental results of the primary side voltages and currents at full load. Three voltage levels (V_{in}, 0 and -V_{in}) are generated on v_{ab} according the states of S_1 and S_4. It is clear that the primary current i_{p1} of the full-bridge converter is reduced to zero at the freewheeling state (v_{ab}=0). Thus, the primary conduction loss at the freewheeling state is improved. Fig. 10 gives the experimental results of the secondary side currents of the full-bridge converter. It can be observed that the rectified voltage v_r is positive voltage instead of zero at freewheeling state. When the diodes D_1 and D_2 are reverse biased, the clamp diode D_a conducts. Fig. 11 shows the test results of the secondary side currents of the half-bridge converter.

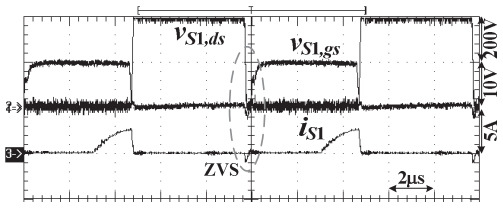

Fig. 5 Measured results of the PWM signals of the leading-leg switch S_1 at 20% load (I_o=8A) and V_{in}=400V.

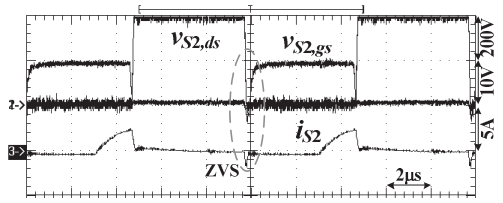

Fig. 6 Measured results of the PWM signals of the leading-leg switch S_2 at 20% load (I_o=8A) and V_{in}=400V.

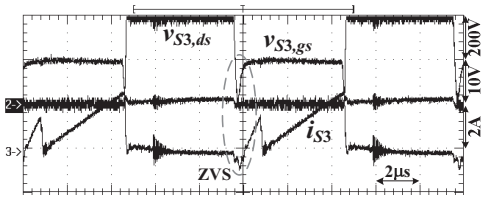

Fig. 7 Measured results of the PWM signals of the lagging-leg switch S_3 at 5% load (I_o=2A) and V_{in}=400V.

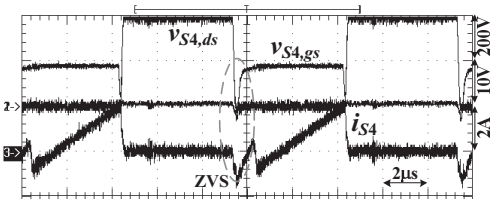

Fig. 8 Measured results of the PWM signals of the lagging-leg switch S_4 at 5% load (I_o=2A) and V_{in}=400V.

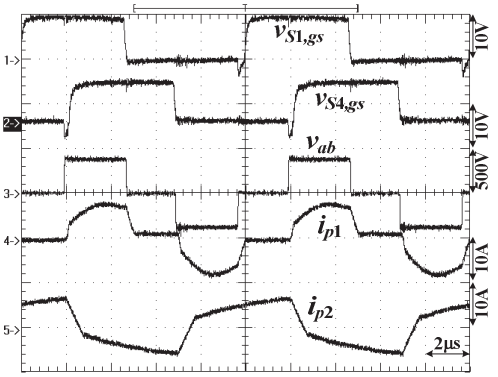

Fig. 9 Measured results of the primary side voltage and current at full load (I_o=40A).

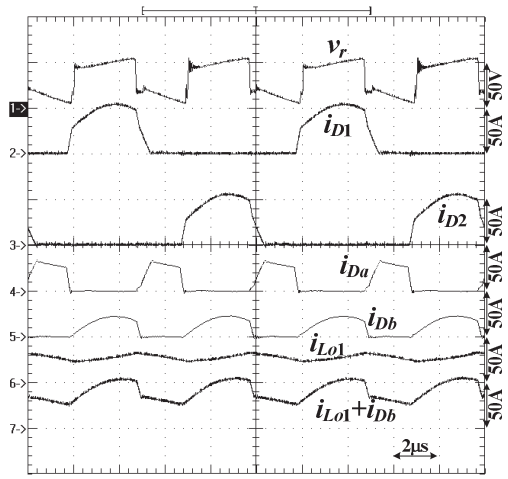

Fig. 10 Measured results of the secondary side currents of the full-bridge converter at full load (I_o=40A).

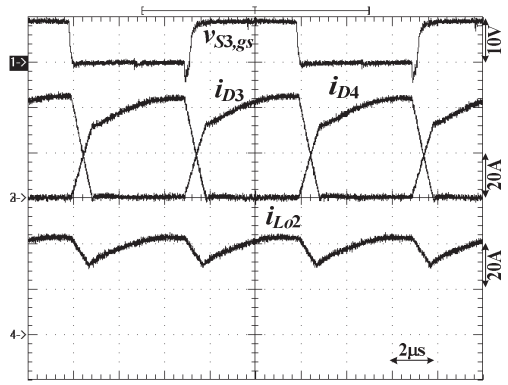

Fig. 11 Measured results of the secondary side currents of the half-bridge converter at full load (I_o=40A).

V. Conclusion

A new DC/DC soft switching converter is presented to achieve the main advantages of wide zero-voltage switching for all switches, low conduction losses at the freewheeling state, less power rating of the passive components and less output inductor size. The adopted circuit includes a full-bridge converter and a half-bridge converter with sharing the lagging-leg switches to extend the ZVS range for all switches. A passive snubber is adopted on the secondary side of the full-bridge converter to reduce the primary current at the freewheeling state due to a positive rectified voltage instead of a zero voltage generated on the secondary side. The effectiveness and performance of the adopted circuit are verified by the experiments with a 1.92 *k*W prototype circuit.

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