出國報告（出國類別：其他-國際會議）

參加「二〇一六年ICEMS國際研討會」出國報告

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摘要

職於 11 月 13~16 日參加二〇一六年 IEEE-ICEMS 電動機與系統國際會議，出席會議之目的是與各國電動機與電力電子方面之專家學者討論電動機製造與控制，電動機動力驅動方面之應用趨勢與介紹個人在此方面之研究成果，並與各國專家學者與廠商交流此方面之發展趨勢。學習各專家學者與業界代表在動力驅動技術、電動車技術與無人駕駛車應用發展。研討會期間與日本及美國專家學者互相討論電力電子技術與電動機驅動等相關問題，以提升在電力電子方面的研究方向。筆者在研討會中發表一篇應用於高壓直流轉換器之電路架構來達到高效率及低損耗之優點，在論文發表時對所提電路架構之優點與其他學者有深入之討論與答辯，此種電路架構具有高效率電路轉換之優點以節省能源損耗，最後利用硬體電路實現來證明所提新型高壓直流電源轉換器之實用性與優越性。參加此次 IEEE-ICEMS 國際研討會獲得很多國外之研究成果，也同時詳細向國外學者介紹台灣之研究近況與績效。

目次

一、 目的

參加二〇一六年IEEE-ICEMS國際研討會之主要目的為: 1.發表研究團隊近兩年在高效率電源轉換之研究成果，2.與各國專家學者討論最新電動機驅動技術之趨勢與發展，3.與國際動力機械專家學者廣泛討論電動車與無人駕駛車技術與趨勢，4.向國際學者介紹台灣研究學者在此方面之研究成果。

二、 過程

二〇一六年IEEE-ICEMS國際電動機與系統研討會在日本/千葉縣召開，會議時間自11月13日至11月16日於千葉縣APA飯店舉行。主辦單位為IEE日本工業應用協會，協辦單位為IEE日本電力與能源協會、韓國電機協會、中國動力技術協會及IEEE工業應用協會。此研討會提供了一個給電機、電子及動力機械學術界能相互交流的環境，並探討創新之發展及電力電子在電動機驅動與控制等相關課題。IEEE-ICEMS國際會議是每年舉辦一次的國際學術研討會，每年會議會在世界各國家輪流舉辦。此次在日本千葉縣舉辦之研討會總共接受之論文篇數約有500篇，共有600多名專家學者參與此研討會。會議中有二場主題演講，主題為JR東日本新幹線鐵路之革新(Mr.Hideyuki Terui)及電動機及驅動之世紀變動(Professor R.D. Lorenz)，這兩場主題演講在11/14日早上10~12於APA飯店演講廳舉行，吸引約600人參與，參加此主題演講之後對於目前世界各國於電動機與驅動方面之趨勢與研究發展有近一步深刻之認識。大會期間共有24個口頭論文發表時段及24個壁報論文發表時段，不論口頭論文發表或壁報論文發表，論文深度都非常好，其中電力轉換器主題有6個時段發表，再生能源主題有4個時段發表，其他為電動機之相關主題有38個時段發表。投稿全文經多位審稿者無記名審查，通過審查共有489篇論文於會議中發表。

11/14日至11/16日參加各場次之論文發表會，11/14日早上參加Mr.Hideyuki Terui及Professor R.D. Lorenz之二場主題演講，主題內容生動活潑受益良多，下午筆者有一篇論文在1:30pm~3:40pm時段以壁報論文發表，論文題目為Analysis of a Zero-Voltage Switching Converter with High Voltage Gain and Low Current Ripple，論文中對於高效率及低損耗的電源供應器有深入討論，電路架構之優勢為具有零電壓切換技術，文章中利用硬體電路實現來證明所提新型電力轉換器之實用性與優越性能，此篇文章獲得日本學者之高度興趣，有日本學者討論與互相交流約有1個小時。筆者告訴日本學者此電路架構可以用於捷運軌道車直流電源系統，因為軌道車之直流電壓高達750V因此筆者使用三階相移電路，利用模組化及三階技術，來達到每個模組電路電流平衡與個別控制之要求，為了達到輸入電容電壓平衡問題，飛輪平衡電容加入在輸入端以便達到次要求。對於筆者之詳細解說與答辯，日本與美國學者感到非常滿意。11/14下午4:00pm~5:45pm參加電力轉換器口頭報告會議，會議中共有3篇論文發表，第一篇論文探討兩相感應電動機之SVPWM控制方式，第二篇論文探討雙向性直流對直流轉換器之控制方式，第三篇論文探討單相功因改善器之控制方式，此三篇論文與會者多人提出多個問題與作者相互答辯。

11/15早上9:30AM~11:00AM參加電力轉換器壁報報告會議，會議中有多篇文章發表電動車驅動技術之改良方法，會議中與作者討論新型電路之優點與缺點，互相交換意見，下午1:00PM~5:40PM參加二場再生能源會議，會議中多篇論文提出再生能源與汽車電池之間的能源轉換技術，讓筆者收穫良多。晚上參加大化主辦之晚宴，晚宴中與日本學者、德國學者、美國學者及中國學者互相交換名片與個人研究領域間之互相交流，晚宴之中與各國學者相談愉快。11/16早上參加一場再生能源會議之後，大會於11點結束。此IEEE國際研討會為一有關電力電子在電動機驅動與控制、綠色能源技術、智慧電網技術與再生能源應用。我國是能源進口國，依賴能源非常嚴重，因此如何節省能源與提高能源利用率是很重要，再生能源之發展可以部份解決此一問題，而如何利用電力電子技術來提高能源轉換之效率是筆者多年來一直努力研究之目標。

三、 心得

ICEMS 國際會議為有關電力電子在電動機驅動與控制、綠色能源技術、智慧電網技術與再生能源應用方面重要會議之一。本次會議共有 489 篇論文。台灣參加師生不多，有清華大學、成功大學、宜蘭大學及國內私立大學教授等人員參加。為提高台灣之學術地位及能見度，仍需科技部與教育部繼續支持。在本次的會議中可以看出論文品質很高，在會議中能認識其他國家的研究學者與業界代表，彼此能交換心得，對於開拓視野、提升研究品質有很大的幫助。會中與各國專家學者交換意見，獲益良多。茲將出席本次會議心得分述如下：

1. 台灣學者與會不多但在論文研究品質上與各國相比較，表現很好。
2. 與各國專家學者交換電源轉換器在電動機應用與再生能源技術。
3. 與日本及美國學者在大會上廣泛互動，作為將來合作之機會。
4. 此次會議中較多研究論文發表集中智慧電動車與再生能源轉換技術。
5. 馬達技術之改良也是此次研討會重點之一。

四、 建議事項

IEEE-ICEMS 國際會議是有關電動機驅動與控制、綠色能源技術與再生能源應用方面的重要國際會議，主要每年在世界各地舉辦之大型國際會議，會議中所發表的論文都相當嚴謹並具有創新性。會議中所發表的論文對電動機驅動與控制之發展有提出多篇重要之研究方向，研討會過程中，發現國內的研究成果優良，研究內容亦受到眾多人的興趣，且整體的素質都受到肯定。大會提供給與會人員研討會相關之文章介紹。由於參與類似的學術性會議非常重要，因此希望政府多鼓勵國內學者積極參與此類型之國際學術會議及加強補助此領域之研究。

五、 附錄

發表論文資料。

Analysis of a Zero-Voltage Switching Converter with High Voltage Gain and Low Current Ripple

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***Abstract*-- An interleaved three-level converter with the new current doubler rectifier is proposed. The main advantages of the proposed converter are zero voltage switching (ZVS) turn-on for all switches, low output ripple current and less voltage stress of the output diodes. Two three-level converters connected in parallel are used to decrease the input current ripple, as well as to reduce the current rating of power switches. At the secondary side, two current doubler rectifiers sharing the same output filter inductors to reduce the output current ripple. The output capacitance of the power switch and the leakage inductance (or external inductance) are resonant at the transition interval so that the power switches can be turned on under ZVS. Experiments with a prototype with 750-800V input and 48V/30A output are provided to verify the theory analysis.**

***Index Terms*—Interleaved PWM, ZVS, Converter.**

I. Introduction

High power high efficiency power converters have been demanded at modern power supply units for the applications of internet of thing (IOT) systems, telecommunication system, and dc-based micro-grid systems. Generally the front-stage of the high power AC/DC converters is a three-phase power factor corrector (PFC) with boost voltage type [1] to achieve the main functions of high circuit efficiency, low line current harmonics, and high input power factor. However, the output voltage of three-phase PFC is higher than 800V for universal three-phase utility voltage. Three-level pulse-width modulation (PWM) converters [2]-[3] have been developed with the main advantages of low voltage rating of power semiconductors, the balance input spilt voltages, and medium power applications. Soft-switching PWM techniques [4]-[5] including zero-voltage switching (ZVS) and zero-current switching (ZCS) have been proposed in three-level converters to reduce the switching losses on power semiconductors due to high switching frequency operation. Phase-shift PWM scheme is one of the most ZVS techniques to improve circuit efficiency in three-level converters. Resonant three-level converters with frequency modulation were discussed in [6]-[7] to realize the ZVS turn-on and possible ZCS turn-off for wide load range. The main drawbacks of the resonant three-level converters are wide switching frequency variations within the whole load range, high circulating current due to low inductance ratio to obtain high voltage gain, and large ripple current on output capacitor. In order to reduce the ripple current for high current output, the current doubler rectifier topology [8] using two filter inductors has been discussed to partially cancel two output inductor currents. Thus, the total output ripple current can be reduced and the size of inductors can be also reduced. Interleaved PWM techniques [9] are the other approaches to increase the total output power, lessen the current rating of power devices, and also reduce the input and output ripple currents. The ripple frequency is two times of switching frequency which can minimize the weight and size of the output filter.

A new interleaved three-level converter with new current doubler rectifier for high voltage applications is presented to realize the main advantages of less current rating of power semiconductors, less output ripple current, ZVS turn-on for all switches, and less filter inductor counts. Two three-level circuits, which are operated by an interleaved PWM to lessen the output ripple current and reduce the current rating of power components, are adopted in the proposed converter. The current doubler rectifier is used at the secondary side to achieve current ripple cancellation. To reduce the filter counts, two filter inductors at the secondary side are both used in each three-level circuits. Finally, experiments are conducted and provided to verify the theoretical analysis of the adopted circuit.

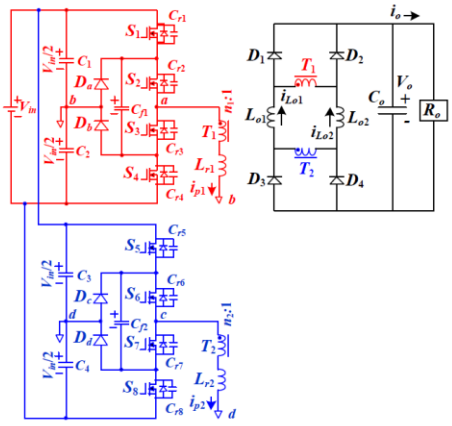


Fig. 1. Circuit diagram of the adopted interleaved three-level converter with new less output inductors.

II. Circuit Diagram

Fig. 1 gives the circuit configuration of the adopted interleaved three-level converter with new current doubler rectifier. The main advantages of the proposed converter are less output inductor components, ZVS operation of power switches and less output ripple current. C_1~C_8 are input split capacitors. The clamped diodes D_a~D_d and the flying capacitors C_{f1} and C_{f2} are adopted to limit the voltage stress of power switches S_1~S_8 at $V_{in}/2$ and to balance the capacitor voltages V_{C1}=..=V_{C8}=$V_{in}/2$. T_1 and T_2 are the isolated transformers to achieve the electrical

isolation and transfer energy to output load. L_{r1} and L_{r2} are the primary leakage (or external) inductances. L_{o1} and L_{o2} are the output inductances and D_1~D_4 are the rectifier diodes. The gating signals of S_5~S_8 are phase-shifted one fourth of switching period with respective to the gating signals of S_1~S_4 in order to reduce the output ripple current. The energy stored on the output inductors L_{o1} and L_{o2} can be reflected to the primary side to help the ZVS operation of S_1~S_8.

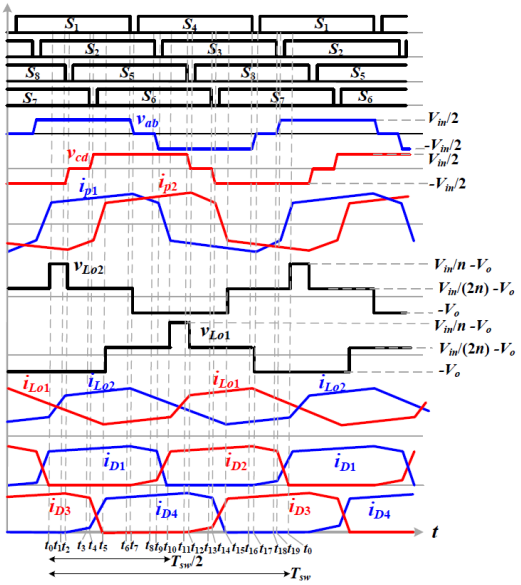


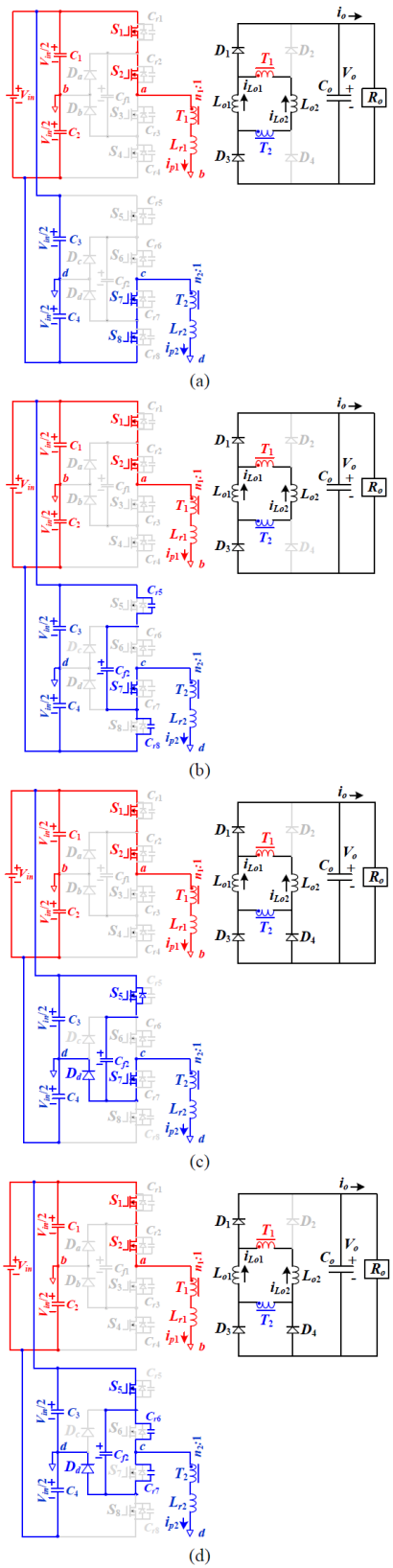
Fig. 2. Main PWM waveforms of adopted three-level converter.

III. Operation Principle

Two three-level converters with the clamped diode and flying capacitor are adopted in the adopted circuit to distribute input power through two converters and reduce the current rating of power semiconductors. The new current doubler rectifier is adopted at the secondary side to reduce the output ripple current. The secondary windings of two transformers are operated in series to reduce the turn ratio of transformers and minimize the primary current stress. The operation principle of the adopted circuit is based on the following assumptions.

(1) The voltages V_{Cf1}=V_{Cf2}=V_{C1}=V_{C2}=V_{C3}=V_{C4}=V_{in}/2;
(2) The output capacitances of switches C_{r1}=..=C_{r8}=C_r;
(3) The output inductances L_{o1}=L_{o2}=L_o;
(4) Power semiconductors are ideal;
(5) T_1 and T_2 are identical n_1=n_2=n and L_{m1}=L_{m2};

Due to the switching states of S_1–S_8, D_a–D_d, and D_1–D_4, twenty operation stages exist in the adopted circuit during one half of switching cycle. Fig. 2 shows the key waveforms of the adopted interleaved PWM circuit during one switching cycle. Two output inductor currents partially cancelled each other. The PWM waveforms for each half switching cycle are symmetrical each other. Thus, only the first ten operation stages shown in Fig. 3 are discussed to simplify the system analysis.



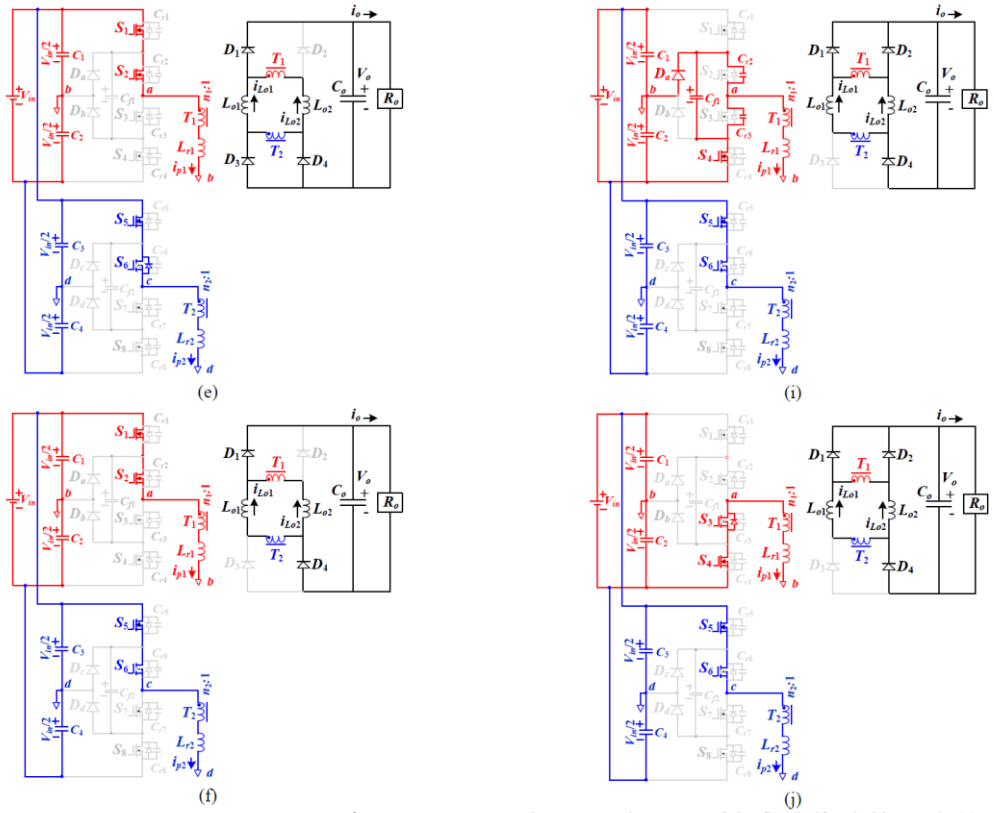


Fig. 3. Operation stages of the first half switching cycle (a) stage 1 (b) stage 2 (c) stage 3 (d) stage 4 (e) stage 5 (f) stage 6 (g) stage 7 (h) stage 8 (i) stage 9 (j) stage 10.

Stage 1 [t_0 - t_1]: At time t_0, the diode current i_{D2} is decreased to zero current. Switches S_1, S_2, S_7 and S_8 are in the on-state and the voltages $v_{ab}=V_{in}/2$ and $v_{cd}=-V_{in}/2$. The secondary winding voltages of T_1 and T_2 are positive and negative, respectively. The output inductor voltages v_{Lo1} and v_{Lo2} are negative and positive, respectively. Thus, the inductor currents i_{Lo1} and i_{Lo2} decrease and increase, respectively. The diodes D_2 and D_4 are reverse biased. The secondary sides of transformers T_1 and T_2 and inductor L_{o2} are connected in series to output load R_o. Energy is transferred to output load through transformers T_1 and T_2 and inductor L_{o2}.

Stage 2 [t_1 - t_2]: S_8 turns off at time t_1. Given that $i_{p1}(t_1)>0$ and $i_{p2}(t_1)<0$, the primary current i_{p2} charges C_{r4} and discharges C_{r5}. Since the energy stored on the output inductor L_{o2} is larger than the energy stored in C_{r5} and C_{r8}, C_{r5} can be discharged to zero voltage at time t_2. This stage ends at time t_2 when V_{Cr8} reaches $V_{in}/2$ and V_{Cr5} reaches zero voltage.

Stage 3 [t_2 - t_3]: V_{Cr5} reaches zero voltage at time t_2. Thus, the clamped diode D_d is conducting. The primary current i_{p2} flows through the anti-parallel diode of S_5. Switch S_5 is turned on at this moment under ZVS. The voltages $v_{cd}=0$ and $v_{Lm2}=0$ such that diode D_4 is forward biased. Thus, the primary current i_{p2} keeps almost constant value and also circulates in the primary side. The output inductor voltages $v_{Lo1}=-V_o$ and $v_{Lo2}=V_{in}/(2n_1)-V_o$ in this stage. Since

$V_{in}/(2n_1)>V_o$, the inductor currents i_{Lo1} and i_{Lo2} decrease and increase, respectively, in this stage.

Stage 4 [t_3 - t_4]: Switch S_7 turns off at time t_3. The primary circulating current $i_{p2}(t_3)$ charges C_{r7} and discharges C_{r6}. If the energy stored in L_{r2} is greater than the energy stored in C_{r6} and C_{r7}, then v_{Cr6} reaches zero at time t_4.

Stage 5 [t_4 - t_5]: V_{Cr6} reaches zero voltage at time t_4. The primary current i_{p2} is negative and flows through the anti-parallel diode of S_6. Therefore, S_6 is turned on at this moment under ZVS. Since D_3 and D_4 are forward biased, the primary magnetizing voltage of T_2 is zero voltage. The primary inductor voltage $v_{Lr2}=V_{in}/2$ and the primary current i_{p2} increases in this stage. The inductor current i_{p2} increases from $-i_{Lo2,max}/n$ to $i_{Lo2,max}/n$ in this stage and ends at time t_5. In this stage, S_5, S_6, D_3 and D_4 are conducting and the secondary side voltage of transformer T_2 is zero voltage. No energy is transferred to output load R_o through transformer T_2. The duty loss in stage 5 is obtained in (13).

$$d_{loss,5}=\frac{\Delta t_{45}}{T_{sw}}\approx\frac{2I_oL_rf_{sw}}{nV_{in}} \tag{1}$$

where T_{sw} and f_{sw} are the switching period and switching frequency, respectively.

Stage 6 [t_5- t_6]: Diode D_3 is reverse biased at time t_5. The primary side voltages $v_{ab}=v_{cd}=V_{in}/2$ and the output inductor voltages $v_{Lo1}=v_{Lo2}=V_{in}/(2n)-V_o$. Thus, the primary currents i_{p1} and i_{p2} and the output inductor currents i_{Lo1} and i_{Lo2} all increase in this stage.

Stage 7 [t_6 - t_7]: S_1 turns off at time t_6. Given that $i_{p1}>0$, C_{r1} is charged and C_{r4} is discharged by i_{p1}. Since the energy stored on the output inductor L_{o2} is larger than the energy stored in C_{r1} and C_{r4}, C_{r4} can be discharged to zero voltage at time t_7. This stage ends at time t_7 when V_{Cr4} reaches zero voltage.

Stage 8 [t_7 - t_8]: At time t_7, V_{Cr4} reaches zero voltage so that D_a is conducting. The primary current i_{p1} flows through the anti-parallel diode of S_4. Therefore, S_4 can be turned on at this moment under ZVS. The primary side voltage $v_{ab}=0$ and $v_{Lm1}=0$ so that diode D_2 is forward biased. In this stage, $v_{Lo1}=V_{in}/(2n_2)-V_o$, $v_{Lo2}=-V_o$, i_{Lo1} increases and i_{Lo2} decreases.

Stage 9 [t_8 - t_9]: Switch S_2 turns off at time t_8. The primary circulating current $i_{p1}(t_8)>0$ will charge C_{r2} and discharges C_{r3}. If the energy stored in L_{r1} is greater than the energy stored in C_{r2} and C_{r3}, then v_{Cr3} reaches zero at time t_9.

Stage 10 [t_9 - t_{10}]: At t_9, V_{Cr3} reaches zero voltage. The primary current $i_{p1}>0$ and flows through the anti-parallel diode of S_3. At this moment, S_3 can be turned on under ZVS. Since D_1 and D_2 are forward biased, the primary magnetizing voltage of T_1 is zero voltage. The primary inductor voltage $v_{Lr1}=-V_{in}/2$ so that the primary current i_{p1} decreases. In this stage, no energy is transferred to output load R_o through transformer T_1. The duty loss in stage 10 is obtained in (2).

$$d_{loss,10}=\frac{\Delta t_{910}}{T_{sw}}\approx\frac{2I_oL_rf_{sw}}{nV_{in}} \tag{2}$$

At time t_{10}, the operation in the first half switching cycle is completed. The operation behaviors of the adopted circuit in the second half switching cycle are symmetrical to the operation principles in the first half switching cycle.

IV. Design Consideration

The charge and discharge times of C_{r1}~C_{r8} in stages 2, 4, 7, and 9 are much less than the other time durations such that these stages are neglected in the following design consideration. Based on the voltage-second balance on output inductors L_{o1} and L_{o2}, the voltage gain is obtained as:

$$\frac{V_o+2V_d}{V_{in}}=\frac{d_{eff}}{n}=\frac{d-d_{loss,5}}{n}=\frac{1}{n}(d-\frac{2I_oL_rf_{sw}}{nV_{in}}) \tag{3}$$

where d_{eff} and d are the effective duty cycle and duty cycle of the voltages v_{ab} and v_{cd} and V_d is the voltage drop on the rectifier diodes D_1~D_4. Given that the allowed maximum duty loss, the necessary primary inductances L_{r1} and L_{r2} can be obtained in (4).

$$L_{r1}=L_{r2}=L_r=\frac{d_{loss,\max}nV_{in,\min}}{2I_{o,\max}f_{sw}} \tag{4}$$

Based on the maximum effective duty cycle, the turn ratio of the transformers T_1 and T_2 is obtained in (5).

$$\begin{aligned}n_1=n_2=n&=\frac{d_{eff,\max}V_{in,\min}}{V_o+2V_d}\\&=\frac{V_{in,\min}}{V_o+2V_d}(d_{\max}-\frac{2I_{o,\max}L_rf_{sw}}{nV_{in,\min}})\end{aligned} \tag{5}$$

For the three-level converter, the ZVS condition of the lagging-leg switches is more difficult to be achieved. The minimum ZVS load condition of the lagging-leg switches is approximately given in (6).

$$I_{o,\min ZVS}\geq 2nV_{in,\max}\sqrt{\frac{C_r}{2L_r}} \tag{6}$$

It is assumed that two output inductor currents are equal to half of the load current $I_o/2$. The ripple currents on the output inductors are expressed in (7).

$$\Delta i_{Lo1}=\Delta i_{Lo2}=\frac{(V_o+2V_d)}{L_of_{sw}}(\frac{3}{4}-d_{eff})=rI_o/2 \tag{7}$$

where r is the current ripple factor of output inductors. Thus, the output inductances L_{o1} and L_{o2} can be derived in (8).

$$L_{o1}=L_{o2}=L_o=\frac{2(V_o+2V_d)}{rI_of_{sw}}(\frac{3}{4}-d_{eff}) \tag{8}$$

The voltage stresses and average currents of the rectifier diodes D_1~D_4 are approximately expressed as:

$$v_{D1,stress}=..=v_{D4,stress}=V_{in,\max}/(2n) \tag{9}$$

$$I_{D1}=..=I_{D4}=I_{o,\max}/2 \tag{10}$$

If the ripple currents of power switches S_1-S_8 are neglected, the root-mean-square (*rms*) currents and the voltage stresses of power switches S_1-S_8 are approximately expressed as:

$$i_{S1,rms}=i_{S4,rms}=i_{S5,rms}=i_{S8,rms}\approx\frac{I_o\sqrt{d_{eff}}}{2n} \tag{11}$$

$$i_{S2,rms}=i_{S3,rms}=i_{S6,rms}=i_{S7,rms}\approx\frac{I_o}{2n\sqrt{2}} \tag{12}$$

$$v_{S1,sterss}=....=v_{S8,stress}\approx V_{in,\max}/2 \tag{13}$$

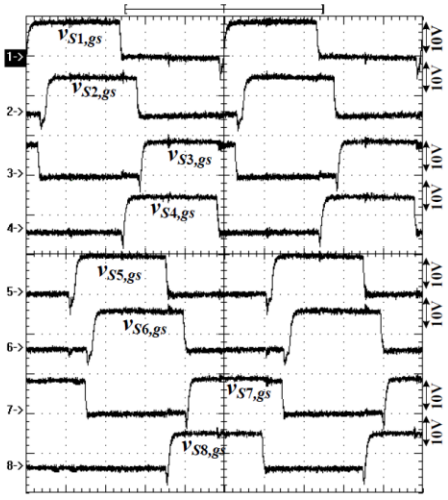


Fig. 4. Measured PWM signals of power switches S_1~S_8 at full load.

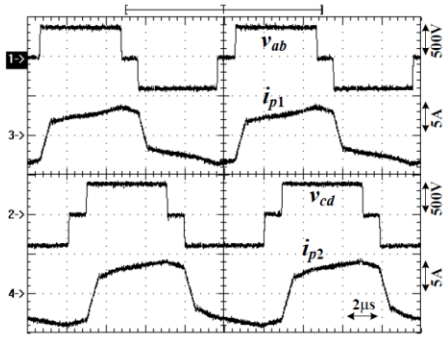


Fig. 5. Measured primary side voltage and currents at V_{in}=800V and full load.

V. Experimental Results

Based on the design considerations in the previous section, the experiments with a laboratory prototype under 750 V to 800 V input, 48 V/30 A output and 100 kHz switching frequency are provided to demonstrate the circuit performance. The circuit parameters of the prototype are n_1=n_2=5.3, L_{m1}=L_{m2}=1.6 mH , L_{r1}=L_{r2}=47 mH , L_{o1}=L_{o2}=44 μH , C_1~C_4:220 μF, C_{f1}=C_{f2}=1 μF, C_o=4000 μF. The experimental waveforms of the gate voltages of S_1~S_8 are given in Fig. 4. The gate voltages of S_5~S_8 are phase-shifted one fourth of switching period with respective to S_1~S_4. The experimental waveforms of the primary side voltages and currents at full load are illustrated in Fig. 5. It can be seen that the primary voltages v_{ab} and v_{cd} are interleaved each other. Similarly, the primary currents i_{p1} and i_{p2} are also interleaved by one fourth of switching period. Fig. 6 gives the experimental waveforms of the gate voltage, drain voltage, and switch current of the leading-leg switches S_1 and S_5 at 40% load and full load under 800 V input. It is clear that the leading-leg switches S_1 and S_5 are all turned on from 40% load to full load. Since the other leading-leg switches S_4 and S_8 have the same operation behavior as S_1 and S_5, switches S_4 and S_8 can be expected to be turned on under ZVS from 40% load. Fig. 7 shows the experimental waveforms of the gate voltage, drain voltage, and switch current of the lagging-leg switches S_2 and S_6 at 40% load and full load. The leading-leg switches S_1 and S_5 are also turned on from 40% load to full load. Figs 8(a) illustrates the experimental waveforms of the primary side voltages and the secondary side currents at full load. Fig. 8(b) shows the output diode current i_{D1}+i_{D2}, capacitor current i_{Co} and the load current. It is clear that two output inductor currents i_{Lo1} and i_{Lo2} are partially cancelled so that the output diode current i_{D1}+i_{D2} is almost constant and the ripple current on the output capacitor C_o is reduced.

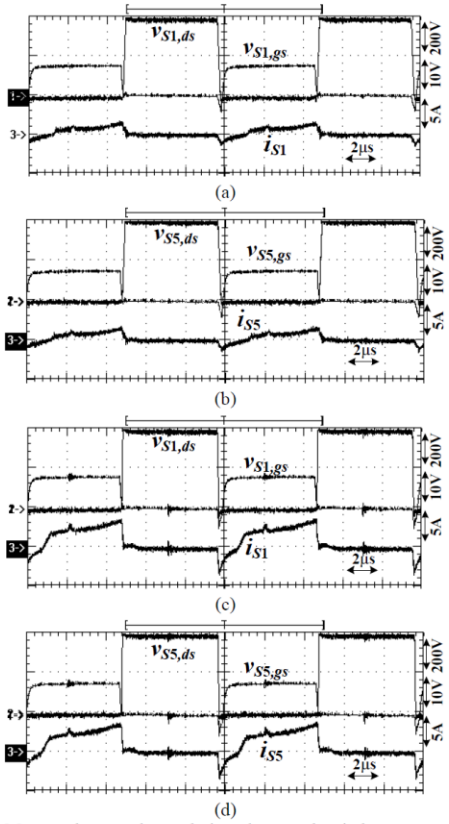
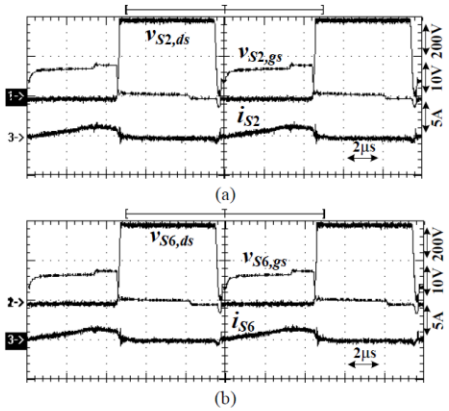


Fig. 6. Measured gate voltage, drain voltage and switch current at the leading-leg (a) S_1 under 40% load (b) S_5 under 40% load (c) S_1 under 100% load (d) S_5 under 100% load.



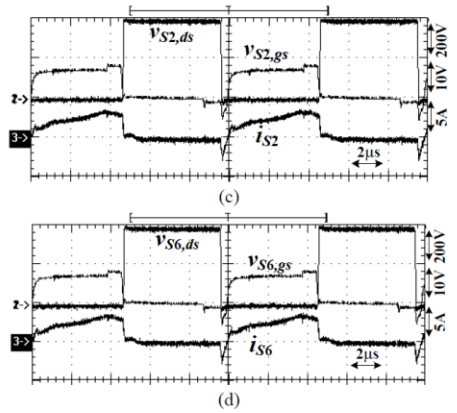


Fig. 7. Measured gate voltage, drain voltage and switch current at the lagging-leg (a) S_2 under 40% load (b) S_6 under 40% load (c) S_2 under 100% load (d) S_6 under 100% load.

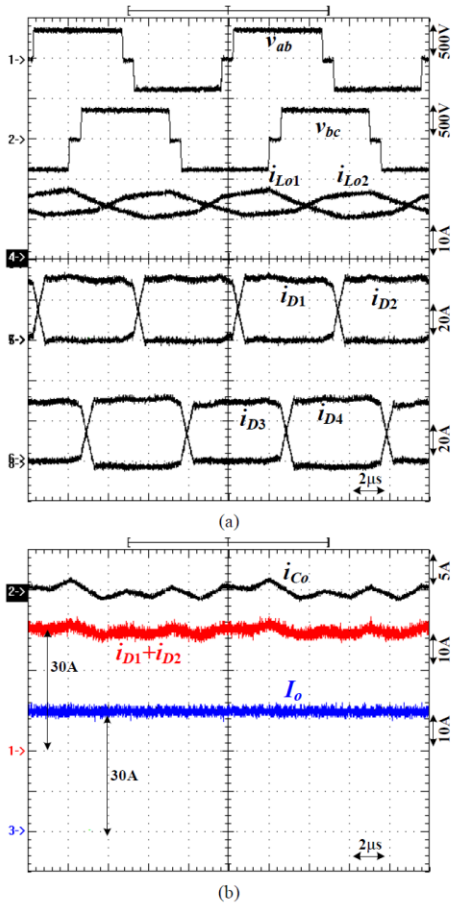


Fig. 8. Measured waveforms at the secondary side (a) the primary side voltages and the secondary side currents at full load (b) the diode current $i_{D1}+i_{D2}$, output capacitor current i_{Co} and load current under full load.

VI. Conclusion

A new interleaved three-level converter with new current doubler rectifier is presented for high voltage applications. Based on the phase-shift PWM scheme, the secondary windings of two transformers can be connected in series or parallel operation to reduce the output ripple current. The output inductor counts are also reduced in the adopted circuit compared to the conventional interleaved current doubler rectifier. Two three-level converters are operated by interleaved PWM scheme to decrease the current rating of active and passive components. In each three-level circuit, the voltage stress of power switches is limited at $V_{in}/2$ by using the diode clamped topology. The flying capacitors are adopted at the primary side to balance two input split capacitor voltages. The adopted converter can achieve ZVS for all power switches from 40% load to full load. In order to further improve circuit efficiency, the synchronous rectifiers instead of rectifier diodes can be used in the proposed converter to reduce conduction losses. Experiments are provided to verify the theoretical analysis.

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