出國報告（出國類別：國際會議）

第十五屆 非揮發性記憶體技術研討會（NVMTS）

服務機關：國立暨南國際大學電機學系
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出國期間：104年10月10日至104年10月15日
報告日期：104年12月29日

摘要

非揮發性記憶體技術研討會（Non-Volatile Memory Technology Symposium）是全球記憶體設計與技術的重要論壇，以加速產品上市的時間，其中需應用到許多科學領域的技術，由設計/設備/製程技術幾大類著手，使縮短產品研發時間。而此次第十五屆非揮發性記憶體技術研討會(NVMTS)是在大陸北京的清華大學（Tsinghua University）舉行，會議日期從2015年10月12日至10月14日止，此次研討會是由北京清華大學、電機電子工程師學會（Institute of Electrical and Electronics Engineers，IEEE）與電子設備學會（Electron Devices Society，EDS）共同舉辦。本屆會議主題包含快閃記憶體（Flash）、磁電阻式記憶體（Magnetoresistive Random Access Memory，MRAM）、相變隨機存取記憶體（Phase Change Memory，PCRAM）、鐵電隨機存取記憶體（Ferro Electric Random Access Memory，FeRAM）等技術探討與研究。此次會議主要任務是希望結合全球專業領域人士，共同關注於新式代記憶體技術，一起改善現今記憶體技術所面臨的難題，並針對相關技術進行交流討論。

關鍵詞: 非揮發式記憶體、快閃記憶體

目次

壹、 參與此次國際會議之目的

非揮發性記憶體技術研討會（Non-Volatile Memory Technology Symposium）是全球記憶體設計與技術的重要論壇，以加速產品上市的時間，其中需應用到許多科學領域的技術，由設計/設備/製程技術幾大類著手，使縮短產品研發時間。而此次第十五屆非揮發性記憶體技術研討會是在大陸北京的清華大學（Tsinghua University）舉行，會議日期從2015年10月12日至10月14日止，此次研討會是由北京清華大學、電機電子工程師學會（Institute of Electrical and Electronics Engineers，IEEE）與電子設備學會（Electron Devices Society，EDS）共同舉辦。本屆會議主題包含快閃記憶體（Flash）、磁電阻式記憶體（Magnetoresistive Random Access Memory，MRAM）、相變隨機存取記憶體（Phase Change Memory，PCRAM）、鐵電隨機存取記憶體（Ferro Electric Random Access Memory，FeRAM）等技術探討與研究。此次會議主要任務是希望結合全球專業領域人士，共同關注於新式代記憶體技術，一起改善現今記憶體技術所面臨的難題，並針對相關技術進行交流討論。

貳、 出國行程及議程

於台灣時間10月10日上午從桃園國際中正機場出發，直飛至大陸的北京首都國際機場，全部航程約莫三個半小時。隨即搭乘機場快軌到轉地鐵至上地站的假日飯店住宿休息。

本次出國行程如下:

10月10日 (六) 桃園中正機場 – 北京首都國際機場

早上到桃園中正機場報到，準備搭機前往北京。

10月11日 (日) 故宮參訪/北京清華大學(會場)

早上搭乘地鐵前往故宮參訪，完畢後為了明日一早能準時參加研討會則搭地鐵到五道口站步行前往北京清華大學參觀。

10月12日 (一) 大會報到/國際會議開幕式

一早從飯店搭乘地鐵至五道口站並步行至清華大學大會會場報到，並參加大會9:00的開幕式。參加完開幕式後，緊接著聆聽美國加州大學的(Yuan Xie)博士演講，內容主要是在闡述現 今最新的記憶體技術與製程方式已及相關技術日後發展。晚上則在大會享用晚餐並張貼此次會議海報並與各國優秀學者討論相關技術。

10月13日 (二) 國際會議

本日上午安排多場演講，主題是在介紹新型存取方式的記憶體，其中以美國科羅拉多大學學者(Carlos A. Paz de Araujo)介紹的相關電子隨機存取記憶體(CeRAMs)最為特

別，此記憶體有絕佳的資料保存力，經高溫測試元件可靠度佳，雖然此技術仍在研發階段，但相信未來此技術有不錯的發展空間。下午的演講內容主要圍繞在非揮發性磁性隨機記憶體(MRAMs)，其原理是利用奈米級磁性結構特有的自旋相關傳輸為基礎的磁電阻效果所得的一種新穎的非揮發性固態磁記憶體，此技術近十年快速發展並進入商品開發階段，相信是未來記憶體產業的主流。另一場演講則是日本東北大學的學者(Tetsuo Endoh)所演講的自旋力矩轉移磁性隨機存取記憶體(STT-MRAM)技術，此技術是前述非揮發性磁性隨機記憶體(ＭＲＡＭｓ)的延伸，其原理則是透過磁阻穿隧接面（Magnetoresistive tunnel Junction， MTJ）進行儲存，利用通入的電流來寫入及抹除數據。寫入及抹除機制則是運用了電子自旋的力矩作用下使磁阻隧道接面（MTJ）的磁化方向發生反轉的工作原理。自旋力矩轉移磁性隨機存取記憶體(STT-MRAM)具有高速度、低延遲時間及良好的使用壽命等優點，且在讀取資料過程中不會造成記憶體資料的破壞，因此被許多人視為未來取代動態隨機存取記憶體(Dynamic Random Access Memory，DRAM)、靜態隨機存取記憶體(Static Random Access Memory，SRAM)的新技術。

10月14日 (三) 國際會議/國際會議閉幕式/晚宴

本日的演講主要是神經形態工程學領域，雖然我對此領域並不拿手，但經由德國的學者(Karlheinz Meier)的發表，對神經形態領域有了初步的認識。此領域還有許多需改進的空間，相信假以時日必定能研發出能精確模擬人腦的晶片(chip)或是電路加以應用造福人群。會議結束後，大會安排搭船前往中央電視台參觀及享用晚餐(晚宴)。

10月15日 (四) 北京首都國際機場 – 桃園中正機場

上午在飯店辦理退房並搭乘飯店的接駁巴士前往北京首都國際機場報到搭機返國。

參、　心得及建議

我覺得參加此次研討會最大的收穫是可以結識到許多來自世界各國的朋友增加自己的溝通力，並以研究當作彼此的共通點，相互切磋討論，讓我有滿滿的收穫。透過此次研討會讓我學習到許多寶貴的研究經驗與技術，例如：如何準備好的國際會議報告；如何傾聽別人報告；如何針對報告發問好的問題；如何結識研究同伴，這些雖然在研究上不是最直接的能力，但長期來看卻是不可或缺的軟實力。最後，謝謝主辦單位北京清華大學、電機電子工程師學會（Institute of Electrical and Electronics Engineers，IEEE）與電子設備學會（Electron Devices Society，EDS）讓我有機會參加此次的研討會，更感謝暨南大學能夠補助經費讓我能有這次寶貴的經驗。

1. **希望能依照不同領域的題目，能有不同的報告場地：**雖然大家研究都是記憶體領域，但還是可以細分為許多項目，所以在此建議主辦單位未來可以將細分的題目獨立出來，以便聽講者可更容易的選擇與自己相關或有興趣的演講題目，如此一來才能讓演講者與聽講者能有更深入的互動。

2. **期盼台灣未來也能多舉辦大型國際研討會：**台灣目前還是鮮少有大型的國際研討會，所以台灣的學生及研究人員往往都須遠赴他國才可發表研究成果，因此期待未來能爭取為大型研討會的主辦地，讓相關人員享有地利之便，讓更多人看見台灣。

肆、附錄

一、 活動照片

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<tr><td>北京清華大學</td><td>清華園</td></tr>
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<tr><td>大會海報合影</td><td>大會開幕式</td></tr>
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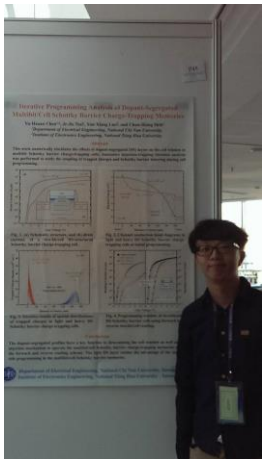
</td><td>  </td></tr>
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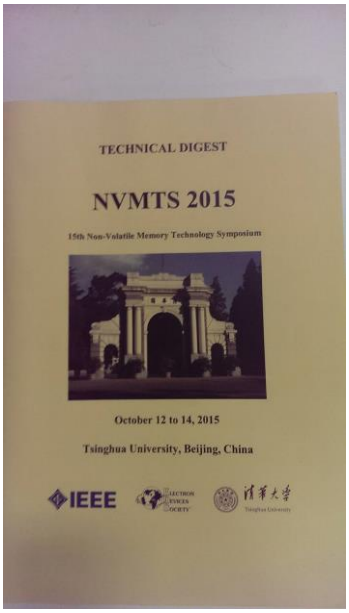	
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	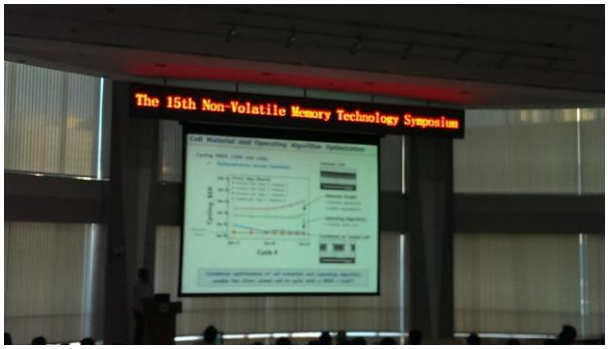
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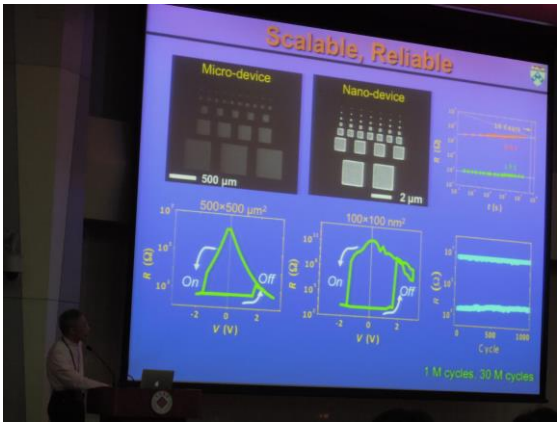	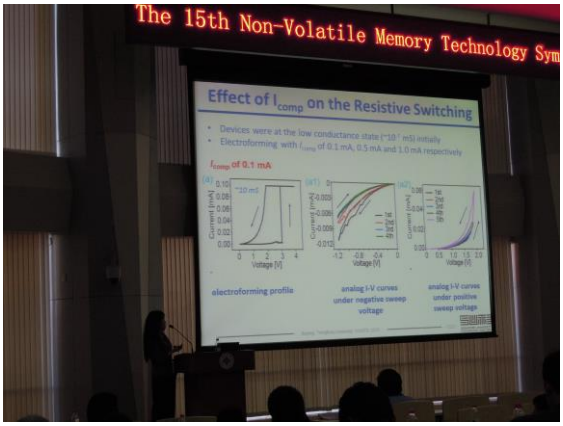
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	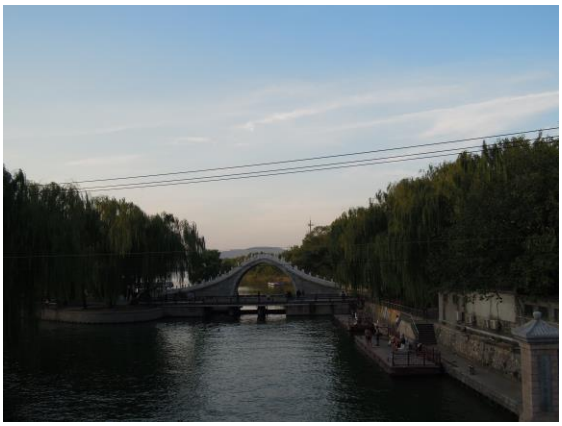
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	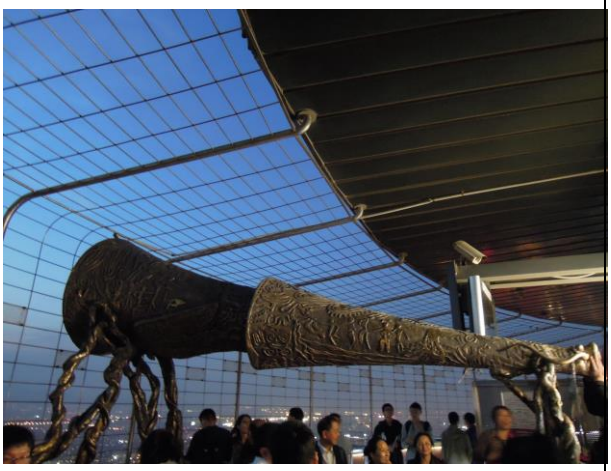
中央電視台 (大會安排)	央視景觀台 (大會安排)
	
中央電視塔 (大會安排)	晚宴會場 (大會安排)

二、 研討會議程

10/12 (Monday)	
08:30 - 08:40	**Opening Ceremony， Chair: Luping Shi** **Welcome and Opening Speech: Professor Qikun Xue, Vice president of Tsinghua University**
08:40 - 09:20	**Keynote: Compact Memristor Models for NonVolatile Memories,** **R. Stanley Williams, Hewlett-Packard Laboratories，USA**
09:20 - 10:35	**Session 1 -Memories , Chair: Jianping Wang** "Memory That Never Forgets: Exploring Nonvolatility of Emerging Memory Technologies for Architecture Design", Yuan Xie, University of California, Santa Barbara，USA. "Memristor-based Random Access Memory/Content-Addressable Memory: The delayed switching could revolutionize nonvolatile memory design", Frank Zhigang Wang, University of Kent, UK. "Neural Networks implementation based on passive memristive crossbars", M. Prezioso , University of California, Santa Barbara, USA.
10:35 - 10:50	**Coffee Break**
10:50 - 12:05	**Session 2 - PCRAM, Chair: Z. M. Sun** " Esigning new Phase Change Materials via Disorder and Stoichiometry ", M. Wuttig , RWTH Aachen University of Technology, Germany. "Direct Observation of Ti-Centered Octahedrons in High-Speed and Low-Energy Ti-Sb-Te Phase Change Material ", Zhitang Song , Shanghai Institute of Micro-system and Information Technology, China. " Multifunctional PCRAM using Topological GeTe/Sb2Te3 Phase-change Superlattice, "J. Tominaga, Nanoelectronics Research Institute, Japan.
12:05 – 14:00	**Take photo /Lunch**

14:00 - 14:40	**Chair: M. Wuttig** **Keynote: Memory Hierarchy on the Future Network,** **Yukihito Oowaki, Semiconductor & Storage Products Company, Toshiba Corp., Japan**
	Session 3 – Systems, Chair: M. Wuttig
14:40 - 15:55	" eNVM Technology Roadmap and eMerging memories development Outlook", Danny Shum , GLOBALFOUNDRIES Singapore Pte, Ltd., Singapore.
	A Ferroelectric-Based Non-Volatile Flip-Flop for Wearable Healthcare Systems," Shintaro Izumi, Kobe University,Japan.
	"Resistive Memory Technology for Embedded and Data Storage Applications", Sung Hyun Jo, Crossbar Inc., USA.
15:55 - 16:10	**Coffee Break**
	Session 4 –RRAM, Chair: Frank Zhigang Wang
16:10 - 17:50	"Scaled-down TaOx ReRAM with high reliability by conductive filament control for embedded application", R. Yasuhara, Panasonic Semiconductor Solutions Co., Ltd., Japan
	"High-density ReRAM for Storage Class Memory", S. Sills, Micron Technology, USA "The Impact of the Electroforming on the Memristor Performance", Zhao Rong, Singapore Univ. of Tech. and Design, Singapore
	"Nanometallic RRAM: Status and Extension of the Concept", I-Wei Chen , University of Pennsylvania, USA.
18：00- 20:30	**Happy Hour and Poster Session, Chairs: Hyunchul Sohn, Huaqiang Wu and Huanglong Li** **Dinner Provided**

10/13 (Tuesday)	
08:30 - 09:10	**Chair: Xiufeng Han** **Keynote: Issues and Prospect of STT-MRAM Development,** **G. H. Koh, Samsung Electronics Co. Ltd, Korea**
09:10 - 10:25	**Session 5 - STT-MRAM, Chair: Xiufeng Han** "Novel Spintronic Devices for Memory and Logic", Jian-Ping Wang, University of Minnesota, USA. " 3D Stackable All-Magnetic MRAM Based on Four Terminal mCell Device", J. G. Zhu , Carnegie Mellon University, Pittsburgh, USA. "STT-MRAM for Nonvolatile Working Memories", Tetsuo Endoh, Tohoku University, Japan.
10:25 - 10:40	**Coffee Break**
10:40 – 12:20	**Session 6 - Emerging memory, Chair: Daisaburo Takashima** "Visualizing CBRAM switching with in situ transmission electron microscopy", B. C. Regan, University of California, Los Angeles (UCLA) ,USA "Nonvolatile Processor Optimization for Ambient Energy Harvesting Scenarios", Vijaykrishnan Narayanan, The Pennsylvania State University, USA. "Impact of Interface Structures on Ferroelectric Resistive Switching Characteristics", A. Sawa, National Institute of Advanced Industrial Science and Technology (AIST), Japan "GeXTe1-X/Sb2Te3 superlattice topological-switching random-access memory", N. Takaura, Hitachi, Ltd., Japan
12:20 - 13:45	**Lunch**

13:45- 14:25	**Chair: Rong Zhao** **Keynote: Spin orbit interaction engineering of magnetic memory for energy efficient electronics systems** **Kang L.Wang, UCLA.USA.**
	Session 7 –Interdisciplinary, Chair: Weisheng Zhao
14:25 - 15:40	"Evaluating Device Parameters of Perpendicular MTJs for Reliable Operation of Embedded STT-MRAM", J.J. Kan, Qualcomm Technologies, USA.
	"Flexible magnetic tunnel junctions and spin-orbit torque MRAM", Hyunsoo Yang, National University of Singapore, Singapore
15:40- 18:30	**Tourism**
18:30- 20:30	**Banquet**

10/14 (Wednesday)	
08:30 - 09:10	**Chair: Yu Wang** **Keynote: Phase Change Memory: The Return of The King** **Hongsik Jeong, Yonsei University.Korea.**
	Session 8 - Neuromorphic Devices, Chair: Yu Wang
09:10 - 10:25	" Brain-Inspired Low Power Neural Networks Using Emerging Resistive Memories as Synapses B.DeSalvo, CEA LETI, Minatec campus, France.
	" ReRAM-based analog synapse for neuromorphic system", H. Hwang, POSTECH, Pohang, South Korea
	"Neuromorphic Crossbars of Memristor Synapses", Kyeong-Sik Min, Kookmin University, Korea.

10:25 - 10:40	**Coffee Break**
	Session 9 - Neuromorphic Systems, Chair: Rong Zhao
10:40 - 11:55	"Study of neuromorphic brain Inspired computing technology", Jing Pei, Tsinghua University, China.
	"Digital Components For Neutral Computing", Lee Wang, FlashSilicon Inc. Taiwan.
	"Hardware Acceleration for Neuromorphic Computing: An Evolving View", Chen Yiran, University of Pittsburg，USA
12:15 - 14:00	**Lunch**
14:00– 14:40	**Chair: Ru Huang** **Keynote 6 Efficient neural hardware for large-scale models,** **Chris Eliasmith, University of Waterloo,Canada**
	Session 10 - Systems, Chair: Ru Huang
14:40 – 15:55	"Towards Flash-based Implementation of Deep Learning networks", F. Merrikh-Bayat, UC Santa Barbara, USA. "Reliability Issues of Oxide Electrolyte Based CBRAM", Ming Liu, the Institute of Microelectronics of the Chinese Academy of Sciences, China "Probable Applications for Phase Change Memory", Chung H. Lam, IBM Watson Research Center, USA.
15:55- 16:40	**Close Ceremony, Chair: Luping Shi** **Close Remark, Professor Kang L. Wang**

Iterative Programming Analysis of Dopant-Segregated Multibit/Cell Schottky Barrier Charge-Trapping Memories

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This work numerically elucidates the effects of dopant-segregated (DS) layers on the cell window in multibit Schottky barrier charge-trapping cells [1]-[3]. Successive injection-trapping iteration analysis was performed to study the coupling of trapped charges and Schottky barrier lowering during cell programming [4], [5].

Fig. 1(a) schematically depicts the structure of a DS-structured Schottky barrier charge-trapping cell, where the multi oxide/nitride/oxide layers of 5/6/7 nm were used to represent typical charge-trapping layers. The DS concentration (N_{ds}) of 10^{19} cm^{-3} and 10^{20} cm^{-3} was typified as the light and heavy profiles. Long-channel cells with uniform profiles were employed to avoid short-channel disturbance. Fig. 1(b) shows the current-voltage curves of DS Schottky barrier cells. The heavy DS cell acquires a better electron on-current and produces a weaker hole current. Fig. 1(c) displays the conduction-band diagrams of light and heavy DS Schottky barrier cells at initial programming. The selection of the heavy or light DS profile determines the injected mechanisms and locations in the DS Schottky barrier cells. Because the drain-side injection generated in heavy DS cells, a higher drain voltage of 6V was employed.

Successive injection-trapping iterations were performed to estimate properly the coupling of the trapped charges and Schottky barrier lowering during cell programming. After each individual programming, the spatial distribution of trapped charges was added in the charge layer according to the lateral spreading of injected currents. Fig. 2(a) presents the calculated results of the spatial distribution of trapped charges after each programming interval. Using the final charge distribution after the successive programming, Fig. 2(b) presents the cell window of programmed DS Schottky barrier cells by the forward and reverse two-bit/cell reading scheme. The light DS Schottky barrier cell shows the excellent immunity of the interference induced from the other bit, whereas the heavy DS cell suffers from considerable distortion caused by the local charges on the opposite site.

The results showed the dopant-segregated profiles have a key function in determining the cell window as well as the injection mechanism to operate the multibit/cell Schottky barrier charge-trapping memories using the forward and reverse reading scheme. The light DS layer retains the advantage of the source-side programming in the multibit/cell Schottky barrier memories.

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References

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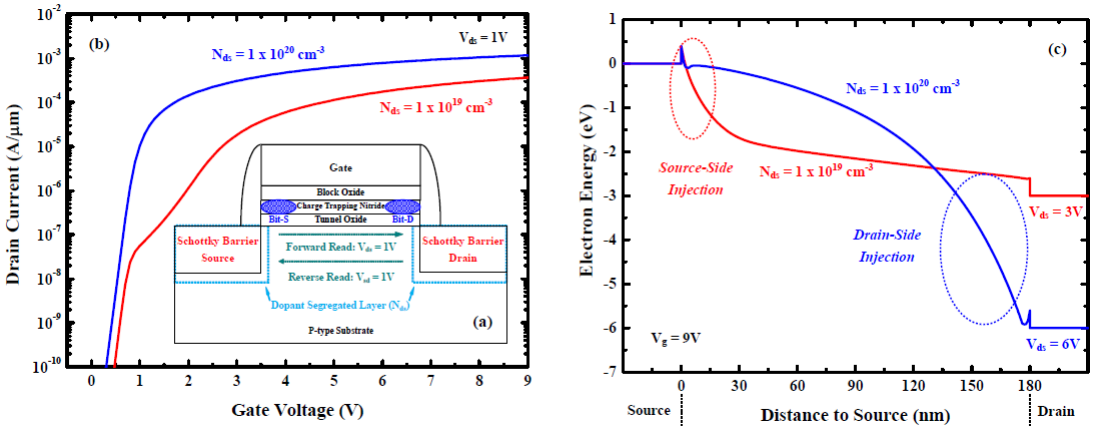

Fig. 1. (a) Schematic structure, and (b) drain current, of a two-bit/cell DS-structured Schottky barrier charge-trapping cell. (c) Channel conduction-band diagrams in light and heavy DS Schottky barrier charge-trapping cells at initial programming.

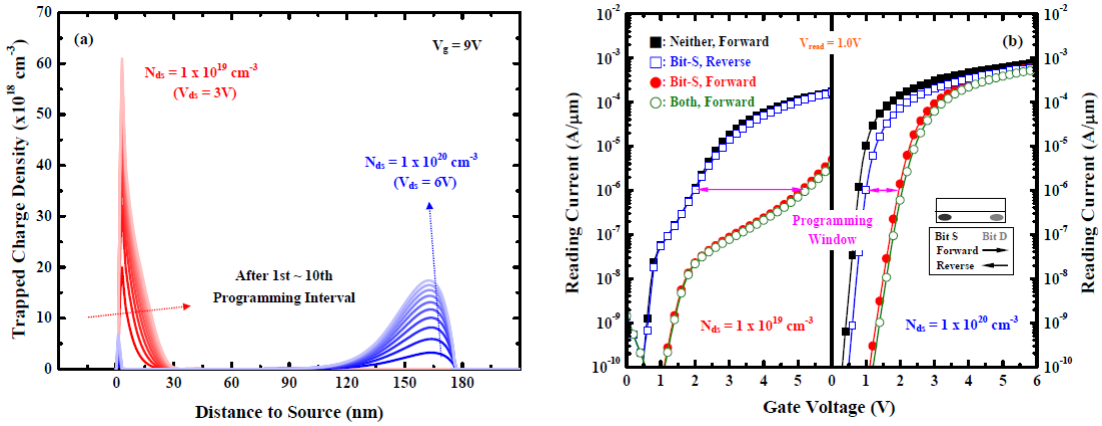

Fig. 2. (a) Iterative results of spatial distributions of trapped charges in light and heavy DS Schottky barrier charge-trapping cells. (b) Programming window of two-bit/cell DS Schottky barrier cells using forward and reverse two-bit/cell reading.