出國報告（出國類別：國際會議 ）

2014 國際氮化物研討會

服務機關：國立中央大學電機系
姓名職稱：辛裕明/教授
派赴國家：波蘭
出國期間：中華民國 103 年 8 月 19 日 至 103 年 08 月 30 日止
報告日期：103 年 09 月 09 日

摘要

參加年度在波蘭樂斯拉夫(Wroclaw)舉行之國際最大的氮化物國際研討會(2014 IWN: International Workshop on Nitride Semiconductors)，並與博士班同學廖文甲發表口頭報告論文一篇(Trap Profile in AlGaN/GaN HFET With Field-Plates Extracted by Transient C-V Measurement)，海報一篇(Self-aligned Ion-implanted W-gate GaN MISFETs with Normally off Operation)。

整個會議區分為四的主要主題，分別是 Growth，Basic Physics & Characterization， Optical Devices，Electronic Devices。筆者因研究領域主要在電子元件，所以主要參加 Electronic Devices 的論文發表討論。

取回大會議程和論文題目摘要一本，隨身碟一個(內含有大會的所有口頭報告跟海報的論文集)。

最後整理口頭報告論文內容，進一步投稿到大會的 Special Issues in *physica status solidi* (a)，題目是 Investigations of Dynamic Performance in AlGaN/GaN HFETs with Field Plates by Stressed C-V and Dynamic On-Resistance Measurements。

目錄

壹、目的

參加年度在波蘭樂斯拉夫(Wroclaw)舉行的國際最大氮化物國際研討會(2014 IWN: International Workshop on Nitride Semiconductors)，與所指導的博士班同學廖文甲共同發表口頭報告論文一篇，與日本法政大學的中村教授合作的(Prof. Nakamura, Hosei University)海報一篇。

口頭報告論文安排在 8 月 27 日早上時段，09:30-09:45 Oral WeEO3，題目是 Trap Profile in AlGaN/GaN HFET With Field-Plates Extracted by Transient C-V Measurement。

海報報告論文安排在 8 月 26 日晚上時段，19:30-21:00 Poster TuEP10，題目是 Self-aligned Ion-implanted W-gate GaN MISFETs with Normally off Operation。

貳、過程

由於國內班機並沒有直飛波蘭樂斯拉夫(Wroclaw)，若是搭長榮飛機直飛到維也納，也沒有聯航的飛機可以轉接前往波蘭樂斯拉夫(Wroclaw)，必須另外購買機票(昂貴，且行李需先領出，再掛送)。經旅行社建議可先飛到鄰近的捷克布拉格，再自行搭火車進出波蘭樂斯拉夫(Wroclaw)。所以依建議改搭阿聯酋航空飛機，先到杜拜機場，再轉阿聯酋航空飛機到捷克布拉格，再搭火車進到波蘭樂斯拉夫(Wroclaw)開會。

開會地點是在波蘭樂斯拉夫(Wroclaw)的百年廳(Centennial Hall 波蘭文：Hala Stulecia)，2006 年，該建築被列為世界文化遺產。由市中心可以搭乘單趟 PLN 3.0 的電車抵達百年廳會場，見到百年廳建築後就可以看到明顯的 IWN 大海報與箭頭方向(如圖一所示)，相當方便。只是要由台灣到波蘭樂斯拉夫(Wroclaw)並不容易。開會地點並不在圖一照片的大廳，而是在附屬的會議廳，但是晚宴則在內舉行。全程有警衛隔離管理，外人沒有開會名牌無法進出，是多年來參加多次的國際會議，首次體會到”被保護隔離”的感覺。

這次開會，乃與所指導的博士班同學廖文甲共同發表口頭報告論文一篇，與日本法政大學的中村教授合作的(Prof. Nakamura Hosei University)海報一篇。

海報報告論文安排在 8 月 26 日晚上時段(如圖二)，19:30-21:00 Poster TuEP10，題目是 Self-aligned Ion-implanted W-gate GaN MISFETs with Normally off Operation。此題目是跟日本法政大學的中村教授合作(Prof. Nakamura, Hosei University)，我團隊分工的部分包括鎢閘極蒸鍍與剝離，

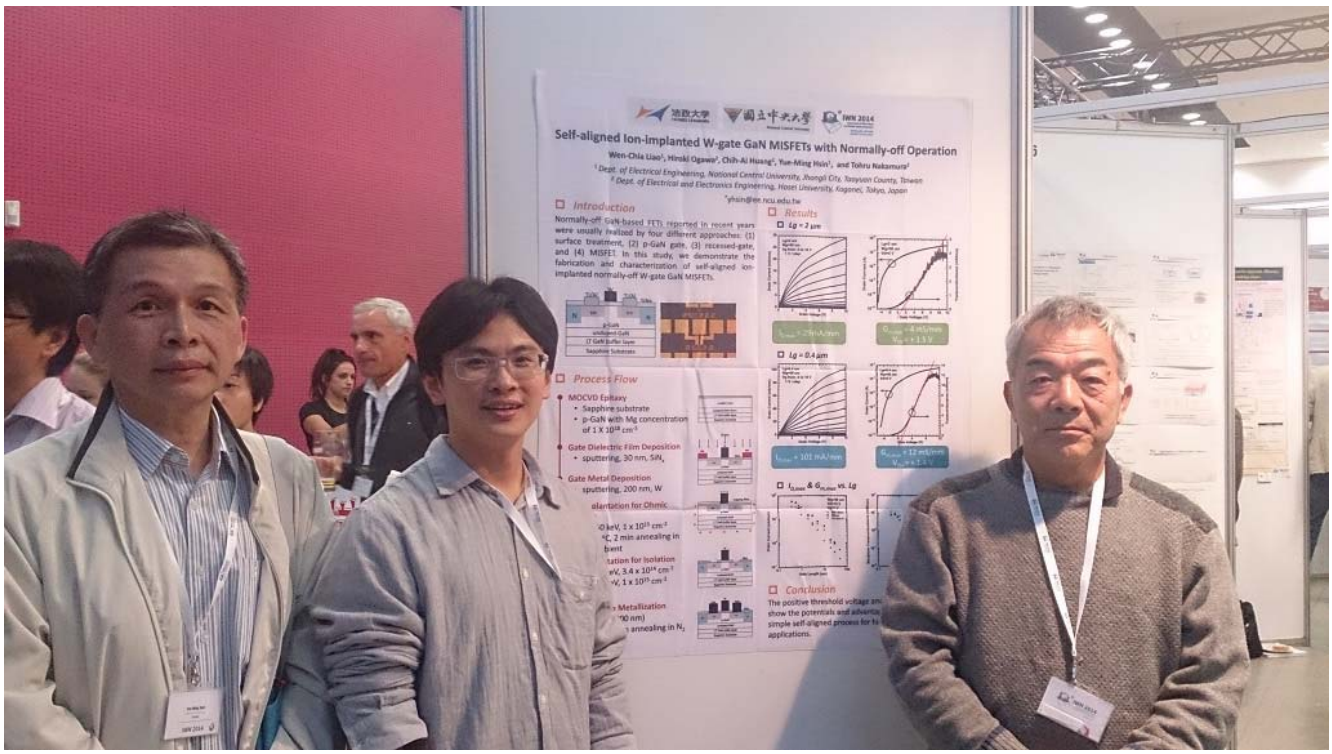
ALD 介電材料沉積，高頻特性測量。參與討論的人許多，提出的問題有，

1. What's the channel mobility?
2. Did lateral diffusion happen after 1100 C annealing process?
3. What is the breakdown voltage?
4. What is the cut-off frequency?
5. What's the resistance in the Ohmic region?

口頭報告論文安排在 8 月 27 日早上時段，09:30-09:45 Oral WeEO3，題目是 Trap Profile in AlGaN/GaN HFET With Field-Plates Extracted by Transient C-V Measurement。緊跟在二位 invited talks 之後，受到矚目。提出的問題包括如何藉由 field plate 設計來改善動態表現，通道電子移動受 field plate 的影響等。

圖一 2014 IWN 開會場地，百年廳(Centennial Hall 波蘭文：Hala Stulecia)

最後整理增加口頭報告論文內容，進一步投稿到大會的 Special Issues in physica status solidi (a)，題目是 Investigations of Dynamic Performance in AlGaN/GaN HFETs with Field Plates by Stressed C-V and Dynamic On-Resistance Measurements。



圖二 2014 IWN 開會海報，與學生廖文甲跟日本法政大學中村教授

參、心得與建議

氮化物國際研討會(2014 International Workshop on Nitride Semiconductors: 2014 IWN)是年度專注在氮化物材料上的材料磊晶、光電與電子元件的相關研究，每二年舉行一次，主要在日本、美國、歐洲的主要城市輪流，上次是在日本的札幌市，下次將在美國舉行。此會議與另一個 International Conference on Nitride Semiconductors (ICNS)相隔年舉行，性質相近，剛好每二年舉行一次。明年的 ICNS 將在中國北京舉行。

整個會議內容除了主要的 plenary lectures 外，區分為四的主要主題，分別是 G: Growth，B: Basic Physics & Characterization，O: Optical Devices，E: Electronic Devices。筆者因研究領域主要在電子元件，所以主要參加 Electronic Devices 的論文討論。以下就所參加的論文發表(包括口頭報告和海報)，簡單列出相關心得：

1. 40 year GaN (Dr. Nakamura) 結論
   甲、GaN on GaN LEDs (2nd Gen in LED) will outtake 1st Gen LEDS in the near future
   乙、Semipolar LD will take over C-plane LD
   丙、GaN substrate is an ultimate substrate
2. 16 years GaN on Si
   甲、主要原因來自於-16.9% GaN on Si lattice mismatch & 54% thermal mismatch
   乙、Min 1990s GaN on Si research effort increases
   丙、Problems: cracking, dislocation, doping (Si doping induces tensile stress)

i. Cracking 可以利用 selective growth, AlN/GaN SL buffer, AlGaN buffer, AlN inter-layer 等方式克服
ii. Dislocation 可以採用 high quality seed layer, strain buffer layer, optimized Al(Ga)N strain engineering layers, SiN in-situ, overgrowth 等方法解決

3. GaN on Si substrate 通常在(111)方向，可以在 CMOS SI 常用的晶片方向(110)嗎?
   甲、LED GaN on Si, 光會被 Si 吸收(>70 % loss), no suitable substrate for HIGH power LED. > remove Si substrate (OSRAM)
   乙、For high-power application: DC-DC, AC-DC, DC-AC converter
   丙、結論:
      i. New devices GaN MEMS on Si,
      ii. low cost high power FET for Power switches,
      iii. GaN on Si substrate is an established but material growth is more demanding than other substrates.
4. Light emitting by nanowire & QD
   甲、Plastic fiber applications 等
   乙、避免在 C-plane 極化，m-plane 沒有極化，e-h recombination rate is better
5. GaN Power Electronics (Ueda 離開 Panasonic 加入 Tokyo Tech)
   甲、Market segments: < 1000V is for GaN (GIT, HFET, MISFET), > 1000V is for SiC (MOSFET, JFET, IGBT)
      i. GaN devices (< 1000V): two major < 100V & 400-1000V
   乙、Normally-off gate injection transistor
      i. FET + Bipolar operation
      ii. Suppressed electron injection back to gate by p+ AlGaN
   丙、Current collapse due to surface traps and bulk traps (thick & epi quality)
      i. Surface traps can be overcome by AlN passivation
      ii. Temperature increases, more current collapse, the reason is due to bulk traps
   丁、FWD diode can be replaced by GIT PN diode, 因為 reverse comduction
   戊、Loss index
      i. On-resistance loss ∝ 1/Wg, loss index: Ron × Wg
      ii. Switching loss ∝ Qsw ∝ Wg, AC loss index: Qsw/Wg
      iii. Gate driver loss ∝ Qg ∝ Wg, GD loss index: Qg/Wg
      iv. Assuming Qsw ∝ Qg => total loss index: Ron × Qg
6. In AlGaN FET future application: fusion of microwave and power
7. AlN/GaN on Si Double Heterojunction HEMT
   甲、Challenges: PAE at > 30 GHz; traps; reliability
   乙、AlN as barrier 6-nm for high breakdown: fmax × BV > 20 THzV (famx > 200 GHz), BV > 100V
   丙、Remove Si substrate under the Gate-drain region to improve breakdown voltage
8. GaN DH-HEMT at high-temperature operation
   甲、DIBL is low, Breakdown Voltage is high
   乙、Narrow channel with DH performs better at H-T
9. C-doped provides excellent BV; Fe-doped provide insufficient BV, which needs for SH structure
10. GaN on Si
   甲、Toward Al-rich AlGaN/GaN HEMT
   乙、On Si sub: 17% lattice mismatch
   丙、Thermal conductivity of Si_GaN << SiC
   丁、Electrical leakage paths
   戊、AlN (2-6nm) can accumulate 2DEG with high carrier density

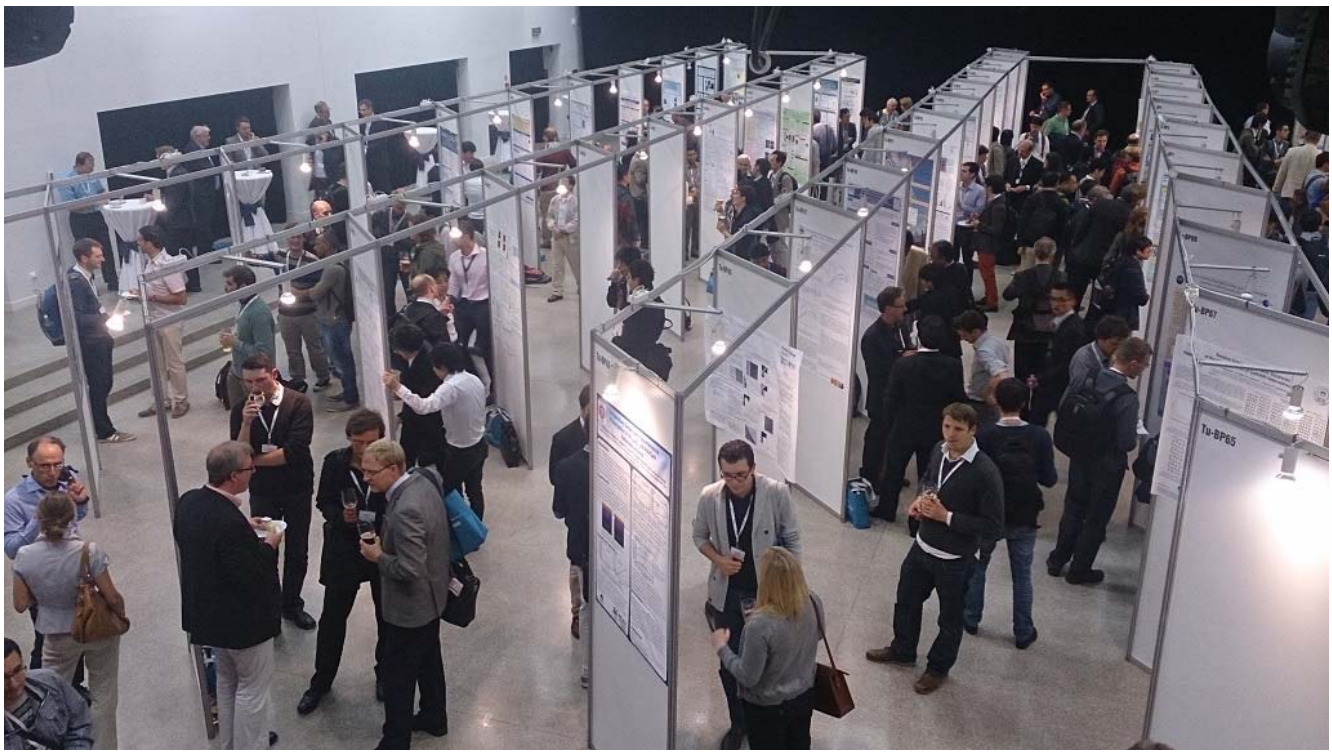
己、GaN 2-nm cap/AlN 3-5nm/GaN 1-um structure

11. 環宇通訊半導體控股股份有限公司(GCS Holdings, Inc)為2010年11月於開曼群島設立之控股公司，並於2010年12月28日與Global Communication Semiconductors, Inc.股東完成換股，因此GCS Holdings, Inc.成為集團之控股母公司。GCS USA於1997年8月成立，獲美國IDM大廠Anadigics簽訂InGaP HBT技術轉移合約，公司主要從事砷化鎵/磷化銦/氮化鎵高階射頻及光電元件晶圓製造代工。集團主要營運地位於美國加州，是美國在射頻和光電元件晶圓領域裡之技術領導者和唯一純專業晶圓製造廠。

    甲、砷化鎵晶圓代工國內外競爭對手包括Triquint、穩懋、聯穎與宏捷科

12. InAlN/GaN HEMT
    甲、Leakage reasons: InAlN barrier: tunneling (1) trap assisted, (2) Fowler-Nordheim tunneling F.N. Tunneling
    乙、Effect of a capping layer: 2-nm or 1-nm GaN cap
    丙、1.5 W/mm at 94 GHz on SiC substrate
    丁、2-nm GaN / 4-nm InAlN/ AlN space 1-nm/ GaN buffer 1um on Si substrate: also show 94 GHz power performance
13. Kevin Chen: E-mode HEMT with digital gate recess
    甲、AlGaN -> oxygen plasma -> HCl etching, then AlGaN & Oxygen plasma …
    乙、Gate recess by RIE + wet etching AlGaN (Oxygen plasma + HCl)
14. Lateral device => premature breakdown => vertical device => reach limit
    甲、George Tech showed InGaN base HBT on sapphire substrate€
        i. Hfe = 75, BV = 60 V, fT = 8 GHz, fmax = 1.8 GHz,
        ii. If on free-standing GaN substrate (n-type GaN)
            1. Beta > 100, BV > 150V
            2. J > 140 kA/cm2
        iii. More In less surface recombination
15. Vertical GaN diode on Si-sub
    甲、Normally-off high BV, better reliability due to high E far from surface.
    乙、But expensive bulk GaN bulk
    丙、No GaN on Si vertical device due to high dislocation
    丁、Surface passivation 要先N2 plasma to reduce leakage
    戊、Should consider the edge termination. High electrical field near gate edge is important.
16. InAlN/GaN on SiC
    甲、Fmax : 300 GHz, load-pull at 94 GHz, 1.5 W/mm (record 1.7 W/mm)
    乙、On Si, at 94 GHz shows 1 W/mm
17. GaN surface with GaOx => high Dit,
    甲、Dielectric/III-N in MIS-HFEMT
    乙、Surface engineering- low dynamic Ron & leakage
    丙、Buffer
    丁、GaO2 removal + N2 plasma (NH3 + Ar) + N2 plasma + ALD + 500C PDA in O2
    戊、AlN: a compelling passivation candidate by ALD

此外海報場地規畫良善，海報欄的空間交錯置放(如圖三所示)，讓參與討論者互動佳，動線也流暢，是少見到的海報欄規畫，值得學習。



圖三 2014 IWN 海報欄的空間交錯置放，互動性佳

氮化物國際研討會(2014 International Workshop on Nitride Semiconductors: 2014 IWN)是年度專注在氮化物材料上的材料磊晶、光電與電子元件的相關研究之最大國際研討會，主要以學校等研發單位參與為主，因非產品導向的研究成果，所以大公司的研發相對少。若是要參加類似的產品研究成果，則應該參加 ISPSD (International Symposium on Power Semiconductor Devices and ICs)為佳。

此次參加的台灣研究團隊並不多,可能是因為開會地點並不容易前往，且報名費、機票與生活費高的原因，在現場曾遇到 3 位老師，清大鄭克勇院長，台大電機吳育任教授，中興大學洪瑞華教授。而中國大陸參與的研究團隊相當多，可以明顯感受到中國大陸在氮化物的光電(LED)和功率(Power)的積極投入研究，參與團隊與經費已經比台灣來得多。且明年將有 2015 ICNS 和 ISPSD 二大功率國際會議在中國大陸舉行，可強烈感受到政府與研究單位的用心。在相關的氮化物(不管是光電，或功率元件)研究成果，將遠超過目前的台灣團隊，值得深思。

肆、附錄

附錄為此次開會所發表的二篇論文內容，包括口頭報告論文：Trap Profile in AlGaN/GaN HFET With Field-Plates Extracted by Transient C-V Measurement，和海報報告論文：Self-aligned Ion-implanted W-gate GaN MISFETs with Normally off Operation

Trap Profile in AlGaN/GaN HFET With Field-Plates Extracted by Transient C-V Measurement

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The AlGaN/GaN heterostructure field effect transistors (HFETs) are promising for high-power applications because they exhibit low on-resistance (R_{on}) and high breakdown voltage [1]. An important requirement in power electronics is maintaining a low R_{on} immediately after switching from a high-voltage OFF state to a low-voltage ON state. Thus, dynamic R_{on} has been studied because R_{on} remains high for a period of time after an OFF-ON switching event. Some research has proposed the degradation in dynamic R_{on} is due to the applied electric field and can be suppressed by using field-plates [2-3]. *C-V* measurement is a powerful method to calculate the interface trap density [4-6]. However, even the trap density and trap level were determined, how the location of traps in HFETs after an OFF-ON switching is unknown. In this study, a methodology involving high voltage capacitances and transient *C-V* characteristics is proposed to determine the trap profile in AlGaN/GaN HFET with field-plates.

FIG.. 1 shows the schematic cross-section of the fabricated AlGaN/GaN MIS-HFET with field-plates. This device is packaged with TO-220, and the substrate is electrically connected to the source. The on-resistance of this packaged device is 10 Ω·mm, and the threshold voltage is -11 V. As the device is biased at V_{gs} of -15 V and V_{ds} of 500 V, the total leakage current is less than 1 mA/mm. High voltage capacitance measurement was carried by Agilent B1505A and C_{gs}-V_{ds}, C_{gd}-V_{ds} and C_{ds}-V_{ds} characteristics were measured at 1MHz. Standard high voltage capacitances were measured at V_{gs} of -15 V and V_{ds} varied from 0 to 400 V. Transient *C-V* characteristics were determined by the two steps process. First, the device was biased at V_{gs} of -15 V and V_{ds} of 400 V for 1 s. Then V_{ds} was immediately switched back to 0 V and increased to 400 V for the *C-V* measurement. Standard and transient *C-V* characteristics are shown in FIG. 2. The difference between standard and transient C_{gd}-V_{ds} curve (FIG. 3) was used to determine the trap profile under gate field-plate. Standard and transient C_{ds}-V_{ds} curve was used to extract the trap profile under the source field-plate (FIG. 4). The extracted trap profiles are shown in FIG. 5. The density of ionized traps shows non-uniform distribution, and is strongly dependent on the locations of field-plates. The maximum density of ionized trap (D_{it}) is 1.3×10^{12} cm^{-2} and located at the gate edge on the drain side. The peak of D_{it} is located at 0.45 μm away from the gate edge. This separation could be attributed to the electrons accelerated by high electrical field towards the drain side before stopping by scattering.

Reference

[1] U. K. Mishra, L. Shen, T. E. Kazior, and Y. F. Wu, *Proc. IEEE* 96, 287 (2008).
[2] W. Saito, T. Nitta, Y. Kakiuchi, Y. Saito, K. Tsuda, I. Omura, , and M. Yamaguchi, *IEEE Trans. Electron Devices* **54**, 1825 (2007).
[3] M. T. Hasan, T. Asano, H. Tokuda, and M. Kuzuhara, *IEEE Electron Device Lett.* **34**, 1379 (2013).
[4] M. Miczek, C. Mizue, T. Hashizume, and B. Adamowicz, *J. Appl. Phys.* 103, 104510 (2008).
[5] S. Huang, Q. Jiang, S. Yang, C. Zhou, and K. J. Chen, IEEE Electron Device Lett. 33, 516 (2012).
[6] Y. Hori, Z. Yatabe, and T. Hashizume, *J. Appl. Phys.* 114, 244503 (2013).

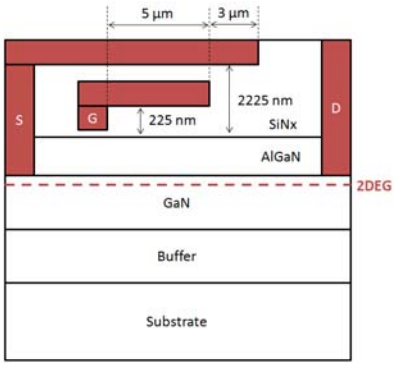


FIG. 1. Schematic cross-section of the AlGaN/GaN MIS-HFET with field-plates.

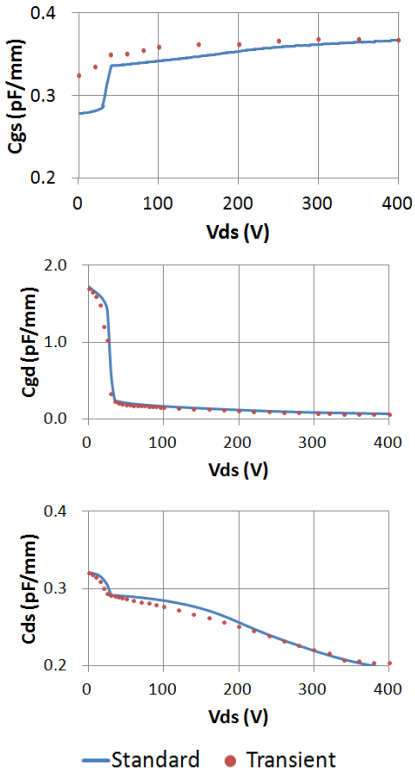


FIG. 2 Standard and transient C-V measurement results.

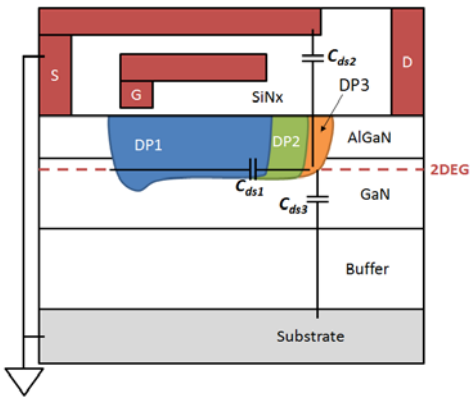
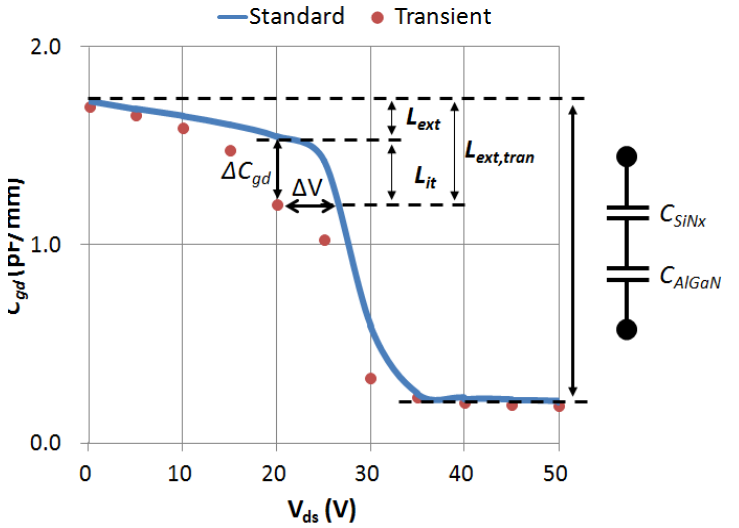
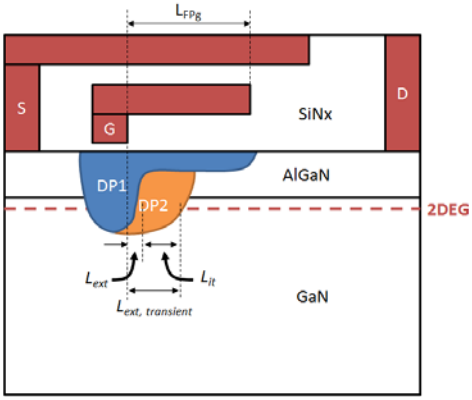


FIG. 4 Depletion extending under source field-plate by varying V_{ds}.





$$L_{ext} = \frac{C_{gd,std}(0V) - C_{gd,std}(Vds)}{C_{gd,std}(0V) - C_{gd,std}(50V)} \times L_{FPg}$$

$$L_{ext,tran} = \frac{C_{gd,std}(0V) - C_{gd,tran}(V_{ds})}{C_{gd,std}(0V) - C_{gd,std}(50V)} \times L_{FPg}$$

$$L_{it} = L_{ext,tran} - L_{ext}$$

$$\Delta C_{gc} = \frac{Q_{it}}{\Delta V}$$

$$D_{it} = \frac{1}{L_{it}} \times \frac{Q_{it}}{q}$$

FIG. 3 Standard and transient C_{gd}-V_{ds} curve for Dit extraction. The cross-section showing additional depletion from ionized traps.

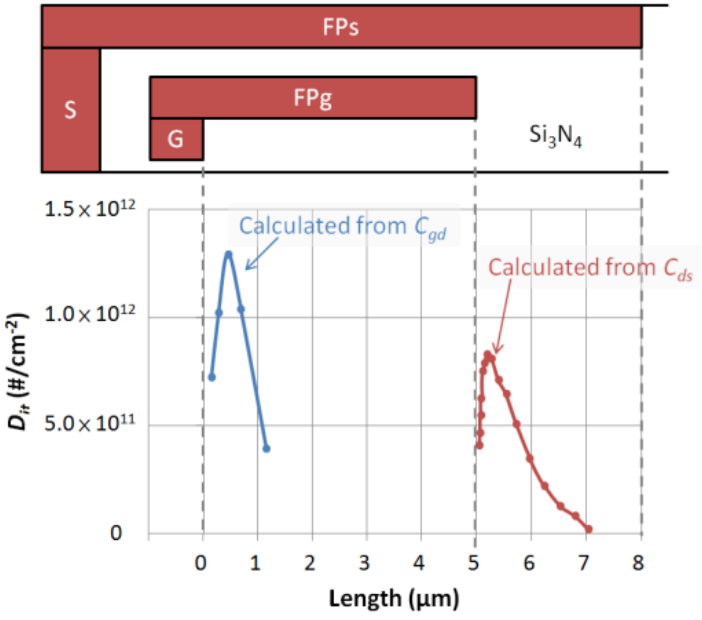


FIG. 5 Trap profile extracted from standard and transient C_{gd}-V_{ds} and C_{ds}-V_{ds} curves.

Self-aligned Ion-implanted W-gate GaN MISFETs with Normally-off Operation

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GaN-based power devices have great potentials and advantages in power switching and RF power applications due to remarkable material properties of GaN, including a wide bandgap, a high breakdown electric field, a high electron saturation velocity, and good thermal conductivity. For realizing low loss and single power switching devices, normally-off devices are required. Normally-off GaN-based FETs reported in recent years were usually realized by four different approaches: (1) surface treatment, (2) p-GaN gate, (3) recessed-gate, and (4) MISFET. In this study, we demonstrate the fabrication and characterization of self-aligned ion-implanted normally-off W-gate GaN MISFETs.

The starting material is a MOCVD grown p-GaN layer with Mg concentration of 1 x 10^{18} /cm^3 on sapphire substrate. A SiN_x film was deposited on p-GaN by sputtering for gate dielectric. Two different thickness of SiN were investigated in this study. The W-gate was formed by sputtering and a subsequent lift-off process. The thickness of the W-gate was designed to be 200 nm, which was thick enough to be a mask in subsequent Si ion implantation. Si ions were implanted into source and drain regions through a SiN_x layer, which were self-aligned to the W-gate. Source and drain regions were obtained by either single or double Si-ion implantation. The 50 nm thick SiO_2 was deposited for passivation by sputtering followed by activation annealing at 1100 ^oC for 2 min in N_2 ambient. After removing the SiO_2, N ions were implanted at the dose of 1×10^{15} /cm^2 and 3.5×10^{14} /cm^2 with energy of 80 and 30 keV, respectively, through a SiN_x layer for device isolation. Source and drain ohmic contacts were formed by depositing Ti/Al (30/200 nm), followed by the thermal annealing at 550 ^oC for 1 min. The sheet resistance in the source and drain regions was 687 ohm/Sq. from the transfer length method (TLM).

Devices with a 0.4-μm gate length and 50-μm width demonstrated a maximum drain current of 102 mA/mm, a maximum transconductance of 12 mS/mm, and threshold voltage of +1.4 V. The on/off current ratio is higher than 10^8. The mobility of 210 cm^2/V-sec was extracted from the transconductance in a 2-μm gate length device.

The positive threshold voltage and high drain current show the potentials and advantages of GaN MISFETs with simple self-aligned process for high voltage and current applications.

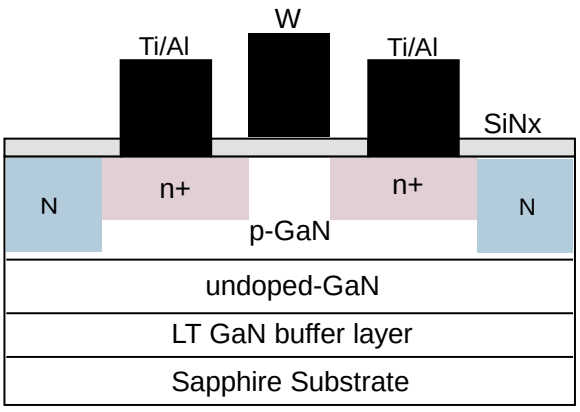

Fig.1 Schematic cross-section of self-aligned W-gate GaN MISFET

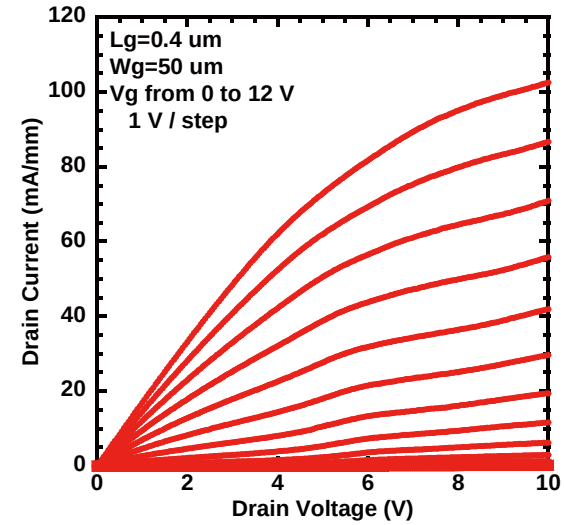

Fig.3 I_D-V_D characteristics of self-aligned W-gate GaN MISFET (30-nm SiN/ Si: 50 KeV)

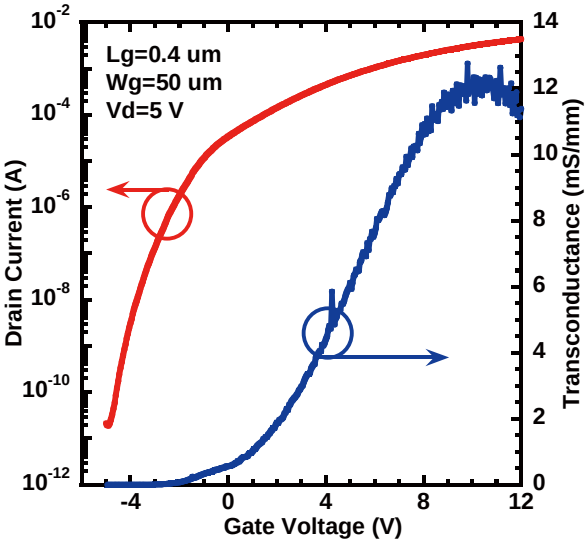

Fig.5 DC transfer characteristics of Self-aligned W-gate GaN MISFET (30-nm SiN/ Si: 50 KeV)

- **Gate Dielectric Film Deposition**
  - SiN 30 nm or 40 nm
- **Gate Metal Deposition**
  - W 200 nm
- **Ion Implantation for Ohmic**
  - Si^+ 50 keV / 1x10^{15} /cm^2 or
  - Si^+ 30 keV / 2.5x10^{14} /cm^2 + 80 keV / 1x10^{15} /cm^2
  - 1100°C 2-min Annealing @N_2 ambient
- **Ion Implantation for Isolation**
  - N: 30 keV / 3.5x10^{14} /cm^2 and 80 Kev /1x10^{15} /cm^2 or
  - N:150 keV / 1x10^{15} /cm^2
- **Source/Drain Metallization**
  - Ti/Al 30/200 nm
  - 550°C 1-min Annealing @N_2 ambient

Fig.2 Process flow of self-aligned W-gate GaN MISFETs

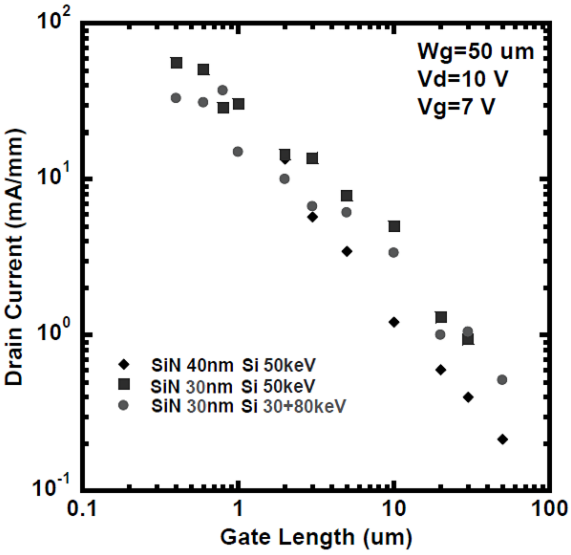

Fig.4 Drain currents versus gate length of fabricated GaN MISFETs at Vg = 7V.

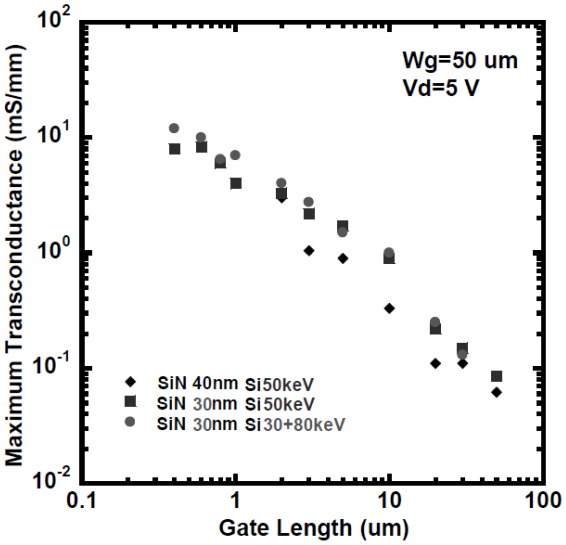

Fig.6 Maximum transconductance versus gate length of fabricated GaN MISFETs.